WR0340

Capacitor-Free, 300mA, Low-Dropout Regulator

1. General Descriptions

The WR0340 series are CMOS-based low-dropout, low-quiescent current linear regulators, offering 300mA with low dropout voltage and high output accuracy. The WR0340 series consist of an accurate voltage-reference block, an error amplifier, a voltage-setting resistor net, a PMOSFET pass device, a thermal-shutdown circuit, and a current limit circuit with short protection.

The WR0340 series is designed with a capacitor-free architecture to ensure stability without an input or output capacitor. A low on-resistance PMOS pass device is equipped for lower dropout voltage. WR0340 also possess the EN function to save more energy and extend the battery life.

The WR0340 series provide an auto-discharging circuit to quickly discharge when disabled.

The WR0340 series are available in standard SOT23-5 package and DFN1*1 package.

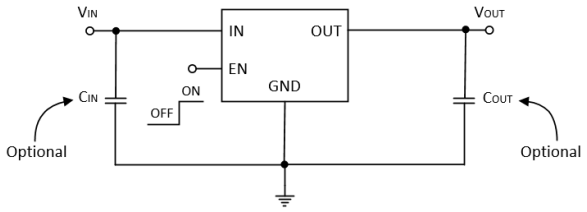
2. Applications

- Constant-voltage power supply for battery -powered device
- Constant-voltage power supply for TV, notebook PC and home electric appliance
- Constant-voltage power supply for portable equipment

3. Features

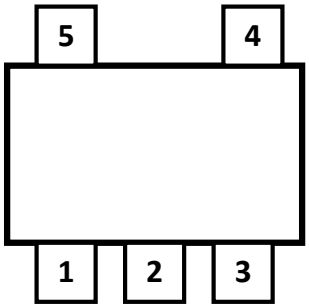
- Wide Input Voltage Range: 1.4V to 5.5V
- Output Current: 300mA
- Output Voltage Range: 1.0V to 3.3V
- Accuracy: 1% typical
- Stable Operation With Capacitor or Not
- Low Dropout: 80mV at 300 mA (V_{OUT}=3.3V)
- Ultra Low I_Q: 34μA
- Excellent Load/Line Transient Response
- Built-in Foldback over current protection
- Built-in Auto-discharging circuit

4. Typical Application

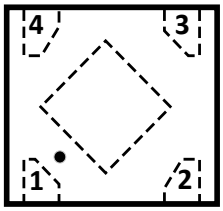


5. Pin Configuration

(Top View)



SOT23-5



DFN-4

6. Pin Description

PIN NUMBER		PIN NAME	I/O	PIN FUNCTIONS
SOT23-5	DFN-4			
1	4	IN	I	Input Voltage
2	2	GND	-	Ground
3	3	EN	I	Enable, Active High
4	-	NC	-	NC
5	1	OUT	O	Output Voltage
		EPAD	-	Exposed pad should be connected directly to the GND pin. Soldered to a large ground copper plane allows for effective heat removal.

7. Absolute Maximum Ratings[1]

PARAMETER		RATING	UNIT
Input voltage range		-0.3 to 6.0	V
EN Input voltage range		-0.3 to V_{IN}	V
Output voltage range		-0.3 to 6.0	V
Maximum output current		300[2]	mA
Power Dissipation PD @T_A = 25ºC	SOT23-5	500	mW
	DFN-4	500	mW
Thermal Resistance, θ_{JA}	SOT23-5	250	℃/W
	DFN-4	250	℃/W
Junction Temperature		150	℃
Lead Temperature Range		260	℃
Storage Temperature Range		-65 to 150	℃
ESD Susceptibility	HBM	±8000	V

Note1: Greater than these given values, the device will be damaged.
Note2: The maximum current that can be output, and guaranteed to work properly.

8. Recommended Operating Conditions

PARAMETER	RATING	UNIT
Input voltage range	1.4 to 5.5	V
EN Input voltage range	0 to 5.5	V
Nominal output voltage range	1.0 to 3.3	V
Output current	0 to 300	mA
Operating temperature range	-40 to 125	℃

9. Electrical Characteristics (V_{IN} = $V_{OUT\ (NOMINAL)}$ + 0.5 V or 2.0 V (whichever is greater), C_{IN} = C_{OUT} = 1μF, Full= -40℃ to 125℃, unless otherwise noted)

SYMBOL	PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{IN}	Input voltage	Full		1.4		5.5	V
V_{OUT}	Output accuracy	Full		0.99 V_{OUT}		1.01 V_{OUT}	V
UVLO	Undervoltage lockout	V_{IN} rising, T_A=25°C			1.3	1.4	V
		V_{IN} falling, T_A=25°C			1.25		
LNR	Line regulation	Δ V_{IN}=V_{IN}(nom) to V_{IN}(nom) + 1, Full			1		mV
LDR	Load regulation[1]	Δ I_{OUT}=1mA to 300 mA, Full			5		mV
V_{DO}	Dropout Voltage[2]	V_{OUT} = 0.98 ×V_{OUT}(nom), I_{OUT}=300mA	V_{OUT} = 1.2 V, Full		250	330	mV
			V_{OUT} = 1.8 V, Full		120	210	
			V_{OUT} = 2.5 V, Full		100	200	
			V_{OUT} = 3.3 V, Full		80	170	
I_{LIMIT}	Output current limit	Full		360		700	mA
I_{OUT}	Maximum output current in the accuracy range[3]	Full		300			mA
I_{SHORT}	Short current[4]	V_{OUT} shorted to GND, T_A=25°C	V_{OUT} = 1.2 V		180		mA
			V_{OUT} = 1.8 V		200		
			V_{OUT} = 3.3 V		280		
I_Q	Quiescent Current	I_{OUT} = 0 mA, Full			34	60	μA
I_{SHDN}	Shut-down Current	V_{EN} = 0V, T_A=25°C			0.1	1.0	μA
PSRR	Power Supply Ripple Rejection	V_{OUT} = 2.5V, I_{OUT}=10mA, T_A=25°C	f=100Hz		68		dB
			f=1kHz		50		
			f=10kHz		40		

Electrical Characteristics (V_{IN} = $V_{OUT\ (NOMINAL)}$ + 0.5 V or 2.0 V (whichever is greater), C_{IN} = C_{OUT} = 1μF, Full= -40℃ to 125℃, unless otherwise noted)

SYMBOL	PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{NO}	Output noise voltage	BW = 10 Hz to 100 kHz, V_{OUT} = 3.3 V, I_{OUT} = 10 mA, C_{OUT}=1μF ,T_A=25°C			140		μV_{RMS}
$V_{EN(HI)}$	EN high threshold voltage (enabled)	Full		0.9			V
$V_{EN(LO)}$	EN low threshold voltage (disabled)	Full				0.4	V
I_{EN}	EN pin current	V_{EN}=5.5V, T_A = 25°C			0.01		μA
R_{DIS}	Output Discharge Resistance	V_{IN}=2.3V， V_{EN}=0V, T_A = 25°C			120		Ω
t_{STR}	Startup time	Time from EN assertion to 98%×V_{OUT}(nom), I_{OUT}= 0mA	V_{OUT} =1.8V, T_A = 25°C		315		μS
			V_{OUT} =2.5V, T_A = 25°C		420		
			V_{OUT} =3.3V, T_A = 25°C		520		
$\frac{\Delta V_{OUT}}{\Delta T_A \times V_{OUT}}$	Output Voltage Temperature Coefficient	I_{OUT}=1mA	Full		50		ppm/ºC
T_{SD}	Thermal shutdown	Shutdown, temperature increasing			160		ºC
		Recover, temperature decreasing			135		ºC

Note1: The Load regulation is measured using pulse techniques with duty cycle < 5%.

Note2: The dropout voltage is defined as (V_{IN}-V_{OUT}) when V_{OUT} is $V_{OUT(NOM)}$*98%.

Note3: Maximum output current is affected by the PCB layout, size of metal trace, the thermal conduction path between metal layers, ambient temperature and the other environment factors of system. Attention should be paid to the dropout voltage when V_{IN}< V_{OUT} + V_{DROP}.

Note4: Short-circuit current limit is RMS value.

Typical Characteristics (V_{IN} = $V_{OUT\ (NOMINAL)}$ + 0.5 V or 2.0 V (whichever is greater), C_{IN} = C_{OUT} = 1μF, Full= -40℃ to 125℃, unless otherwise noted)

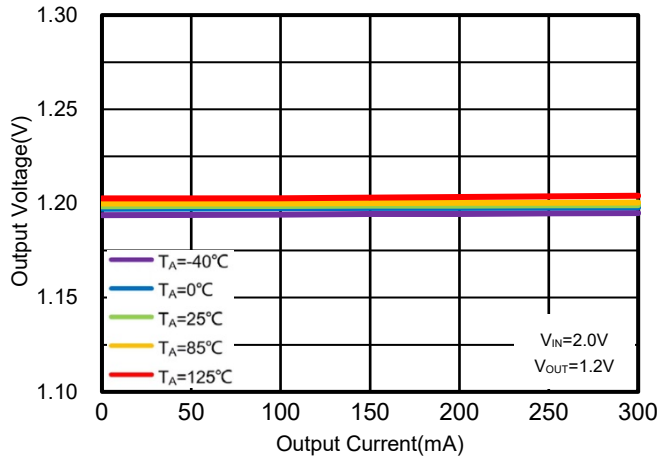


Figure 1. WR0340-12A50R
Load Regulation vs I_{OUT} & Ambient Temperature

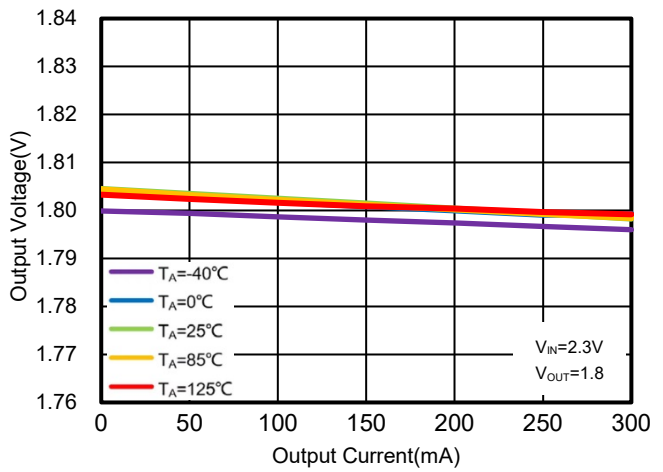


Figure 2. WR0340-18FF4R
Load Regulation vs I_{OUT} & Ambient Temperature

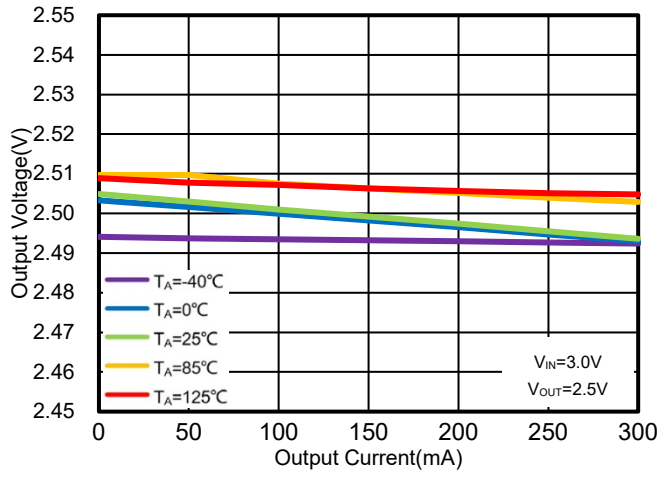


Figure 3. WR0340-25A50R
Load Regulation vs I_{OUT} & Ambient Temperature

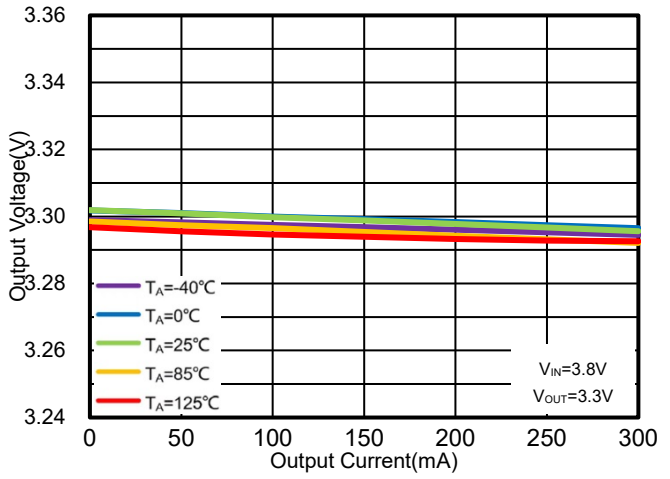


Figure 4. WR0340-33FF4R
Load Regulation vs I_{OUT} & Ambient Temperature

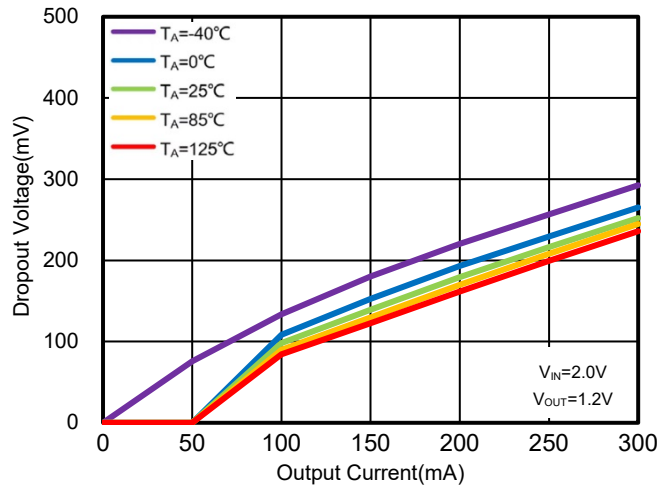


Figure 5. WR0340-12A50R
Dropout Voltage vs I_{OUT} & Ambient Temperature

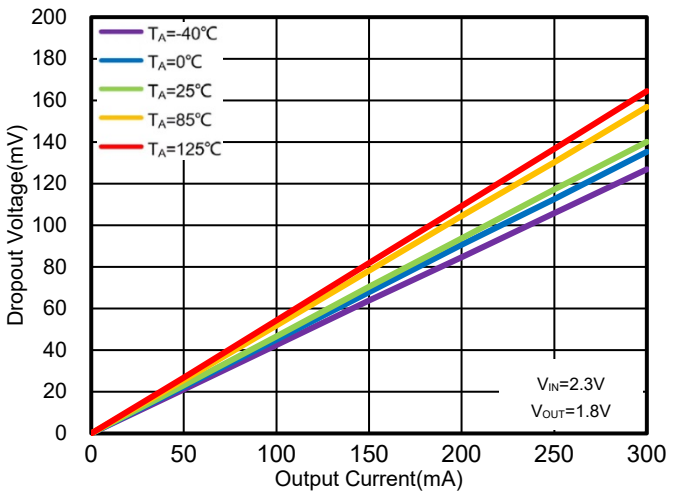


Figure 6. WR0340-18FF4R
Dropout Voltage vs I_{OUT} & Ambient Temperature

Typical Characteristics (V_{IN} = $V_{OUT\ (NOMINAL)}$ + 0.5 V or 2.0 V (whichever is greater), C_{IN} = C_{OUT} = 1μF, Full= -40℃ to 125℃, unless otherwise noted)

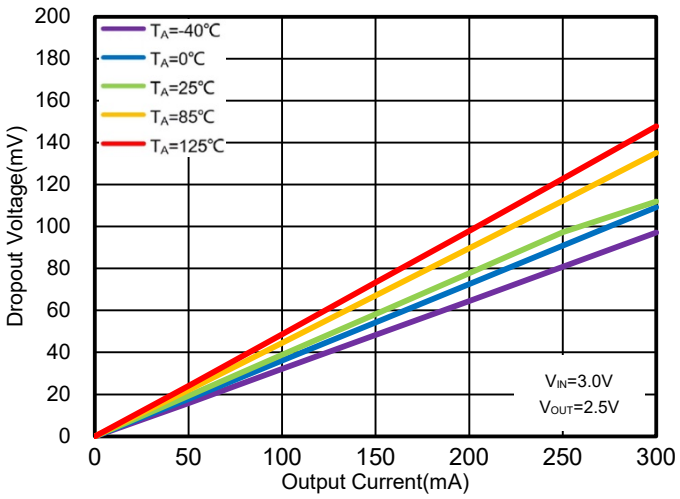


Figure 7. WR0340-25A50R
Dropout Voltage vs I_{OUT} & Ambient Temperature

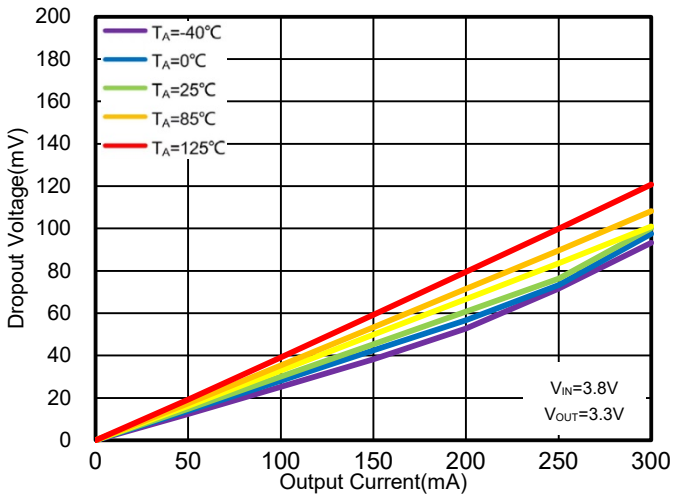


Figure 8. WR0340-33FF4R
Dropout Voltage vs I_{OUT} & Ambient Temperature

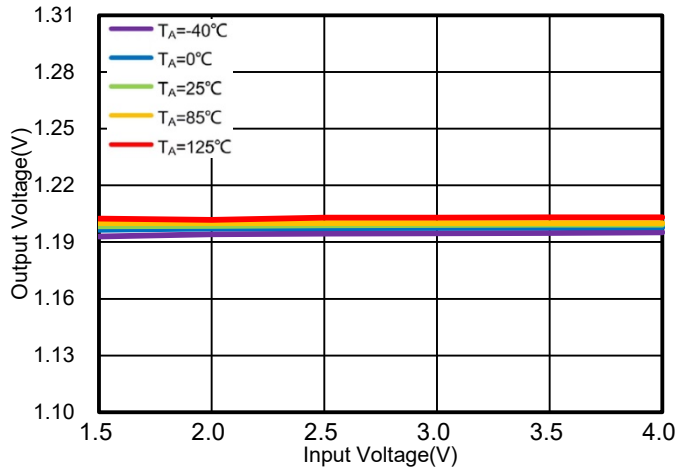


Figure 9. WR0340-12A50R
Regulation vs V_{IN} (Line Regulation) & Ambient Temperature

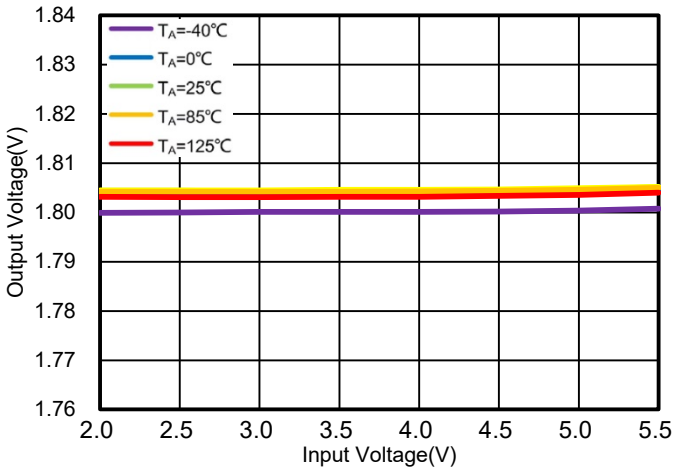


Figure 10. WR0340-18FF4R
Regulation vs V_{IN} (Line Regulation) & Ambient Temperature

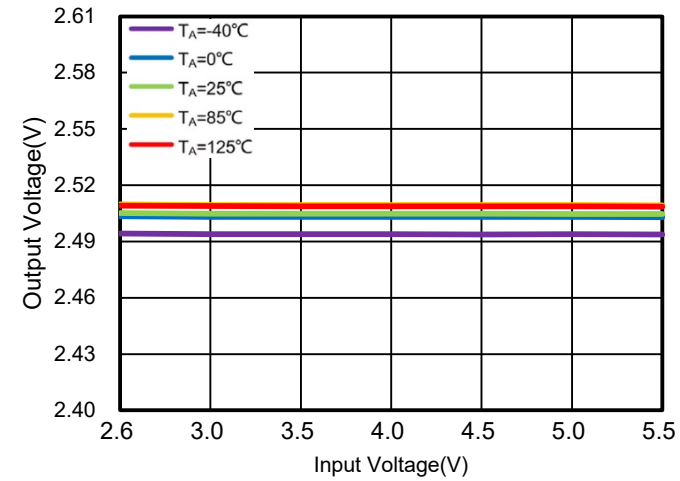


Figure 11. WR0340-25A50R
Regulation vs V_{IN} (Line Regulation) & Ambient Temperature

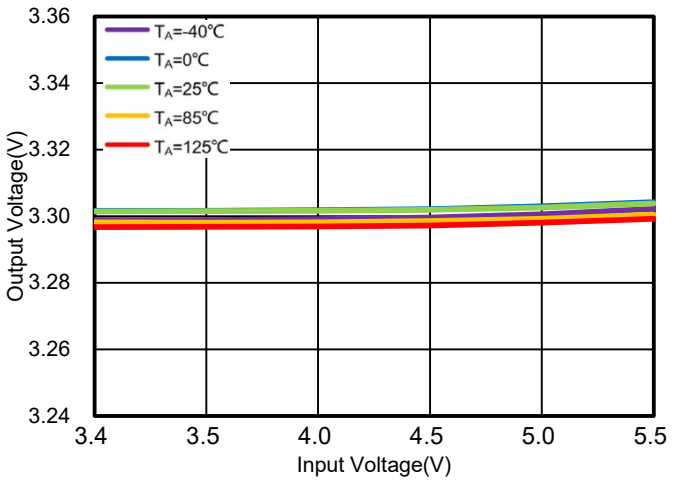


Figure 12. WR0340-33FF4R
Regulation vs V_{IN} (Line Regulation) & Ambient Temperature

Typical Characteristics (V_{IN} = $V_{OUT\ (NOMINAL)}$ + 0.5 V or 2.0 V (whichever is greater), C_{IN} = C_{OUT} = 1μF, Full= -40℃ to 125℃, unless otherwise noted)

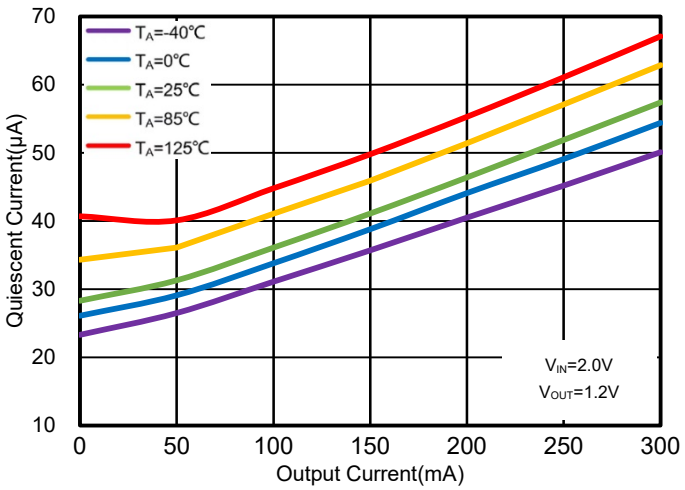


Figure 13. WR0340-12A50R
Quiescent Current vs I_{OUT} & Ambient Temperature

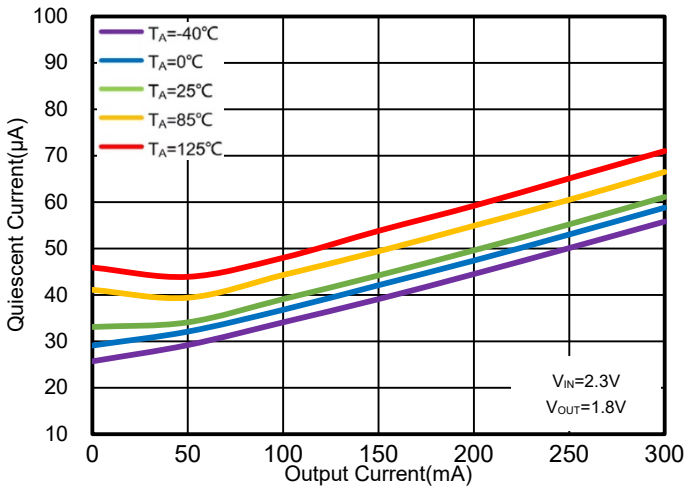


Figure 14. WR0340-18FF4R
Quiescent Current vs I_{OUT} & Ambient Temperature

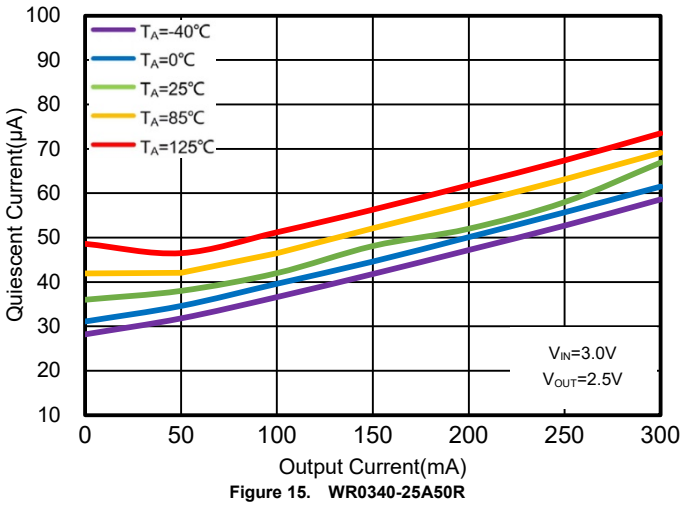


Figure 15. WR0340-25A50R
Quiescent Current vs I_{OUT} & Ambient Temperature

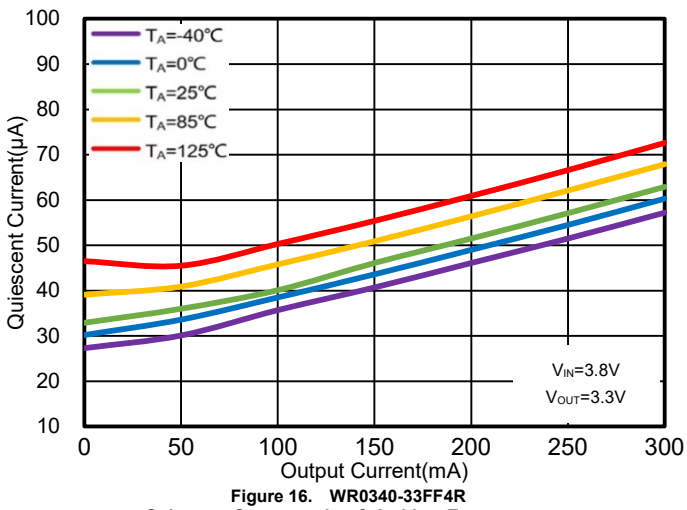


Figure 16. WR0340-33FF4R
Quiescent Current vs I_{OUT} & Ambient Temperature

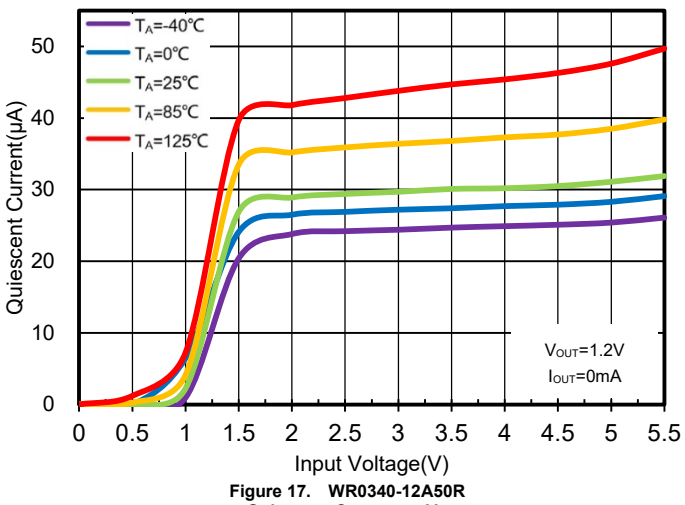


Figure 17. WR0340-12A50R
Quiescent Current vs V_{IN}

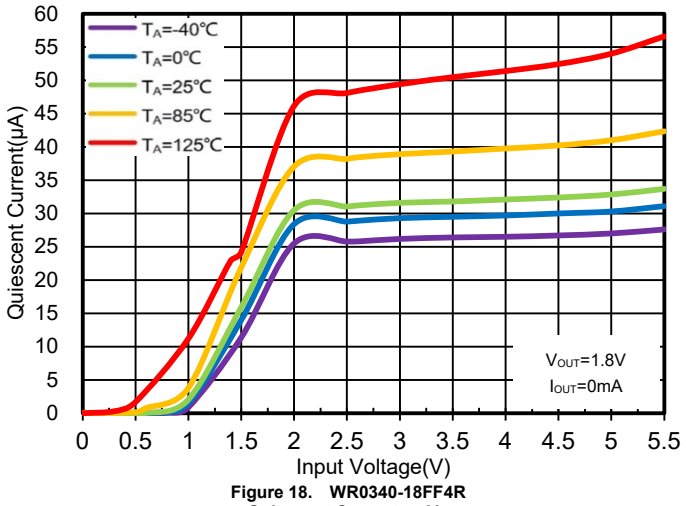


Figure 18. WR0340-18FF4R
Quiescent Current vs V_{IN}

Typical Characteristics (V_{IN} = $V_{OUT\ (NOMINAL)}$ + 0.5 V or 2.0 V (whichever is greater), C_{IN} = C_{OUT} = 1μF, Full= -40℃ to 125℃, unless otherwise noted)

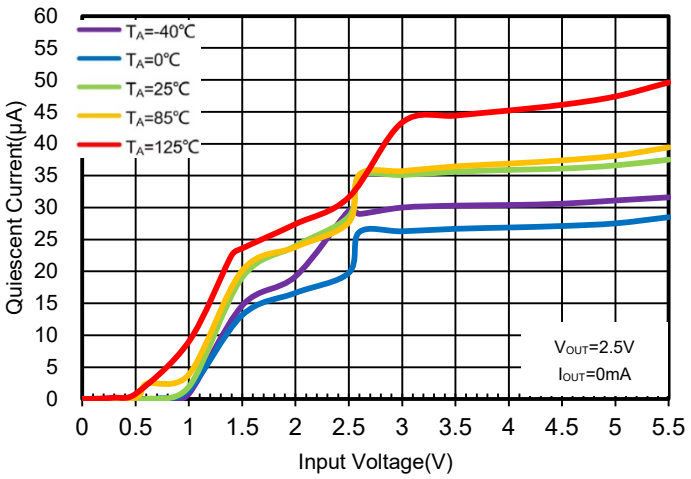


Figure 19. WR0340-25A50R
Quiescent Current vs V_{IN}

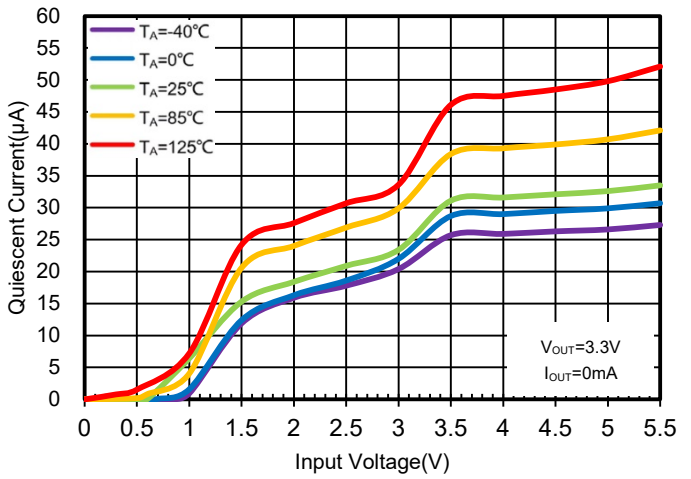


Figure 20. WR0340-33FF4R
Quiescent Current vs V_{IN}

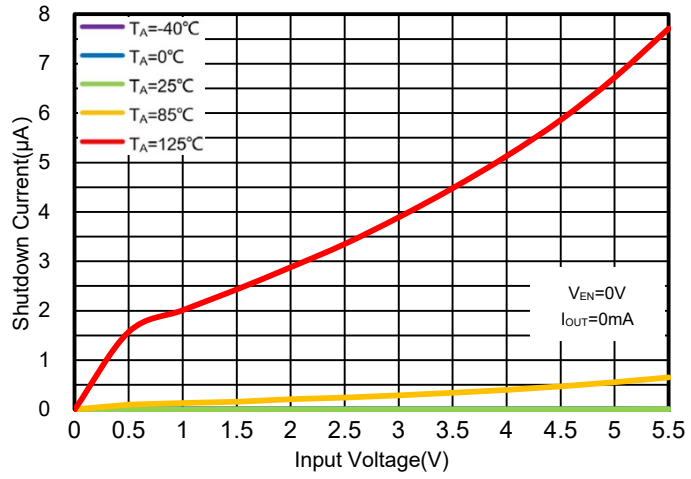


Figure 21. WR0340-12A50R
Shutdown Current vs V_{IN} & Ambient Temperature

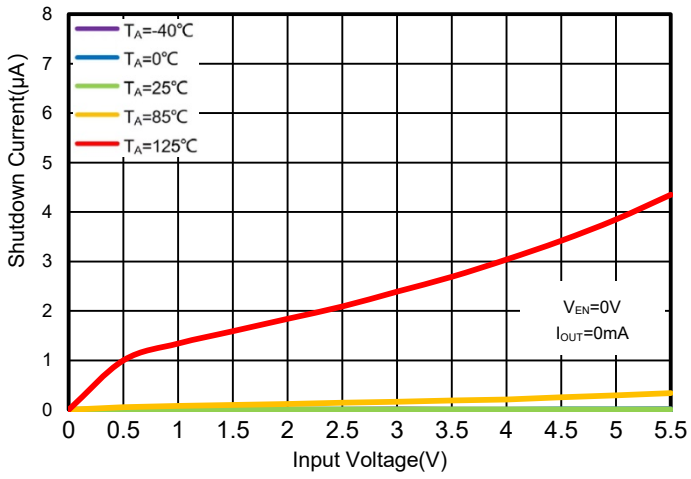


Figure 22. WR0340-18FF4R
Shutdown Current vs V_{IN} & Temperature

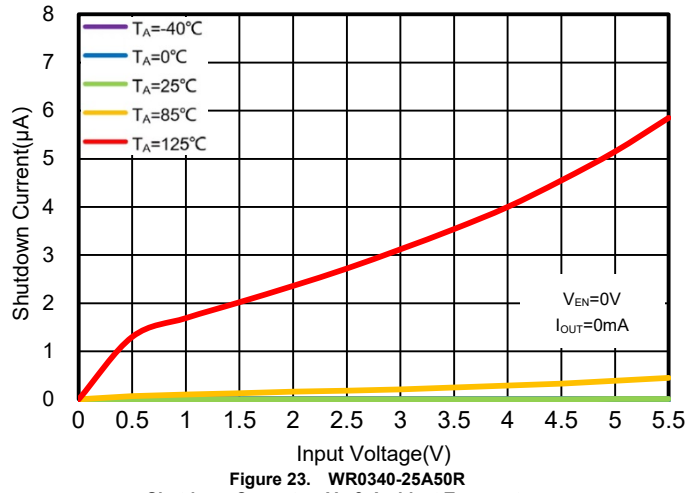


Figure 23. WR0340-25A50R
Shutdown Current vs V_{IN} & Ambient Temperature

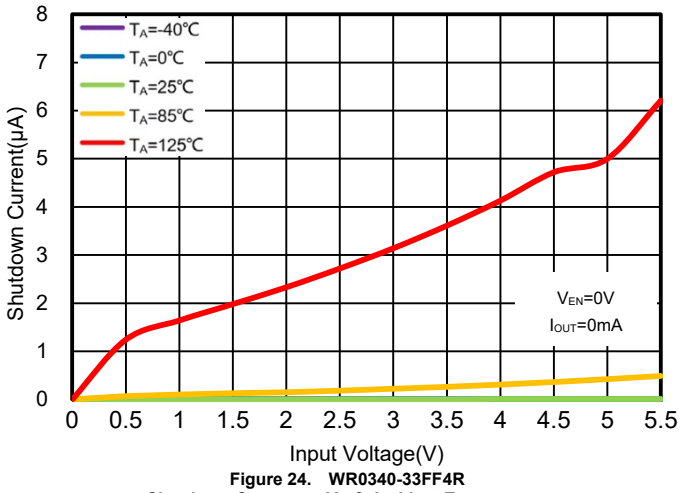


Figure 24. WR0340-33FF4R
Shutdown Current vs V_{IN} & Ambient Temperature

Note: The curves for temperatures of -40°C, 0°C, 25°C in figures 21 to 24 overlap each other.

Typical Characteristics (V_{IN} = $V_{OUT\ (NOMINAL)}$ + 0.5 V or 2.0 V (whichever is greater), C_{IN} = C_{OUT} = 1μF, Full= -40℃ to 125℃, unless otherwise noted)

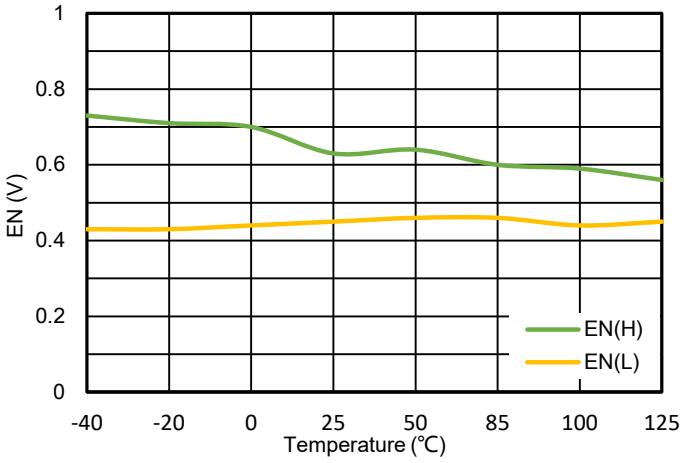


Figure 25. WR0340-12A50R
Enable Threshold vs Ambient Temperature

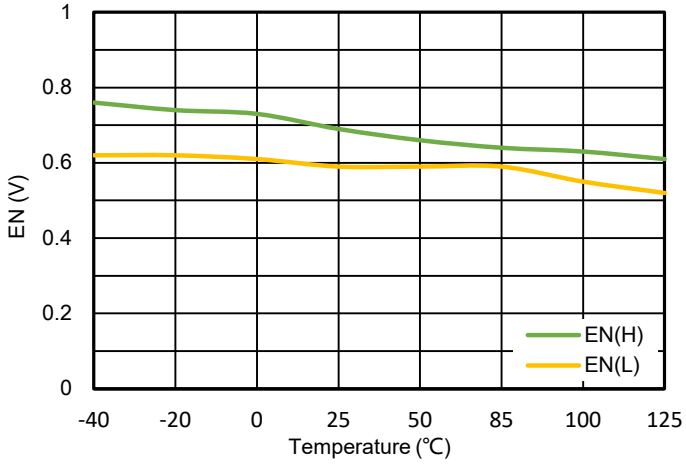


Figure 26. WR0340-18FF4R
Enable Threshold vs Ambient Temperature

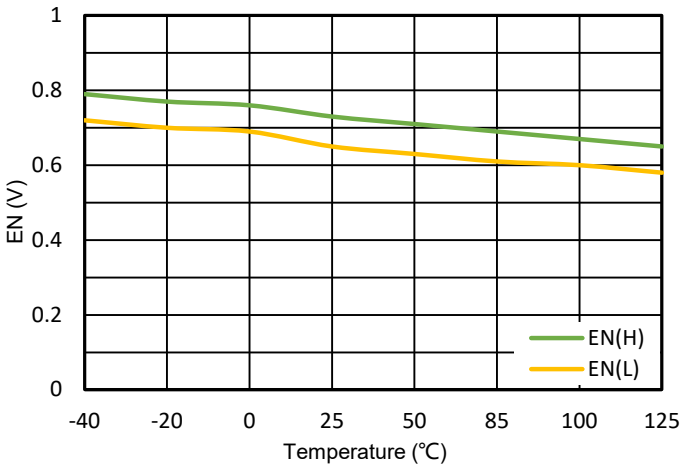


Figure 27. WR0340-25A50R
Enable Threshold vs Ambient Temperature

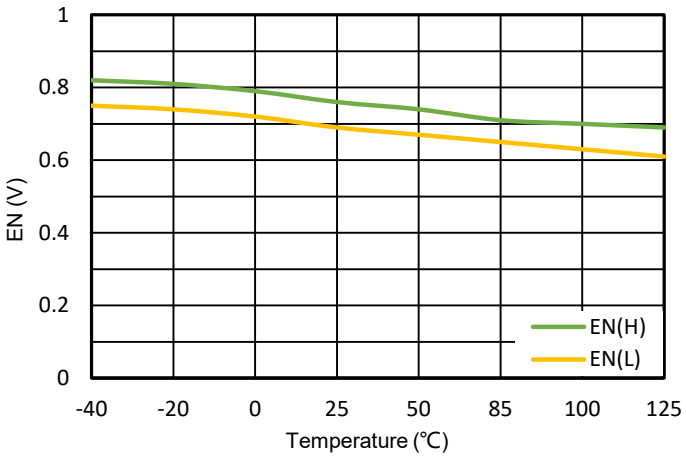


Figure 28. WR0340-33FF4R
Enable Threshold vs Ambient Temperature

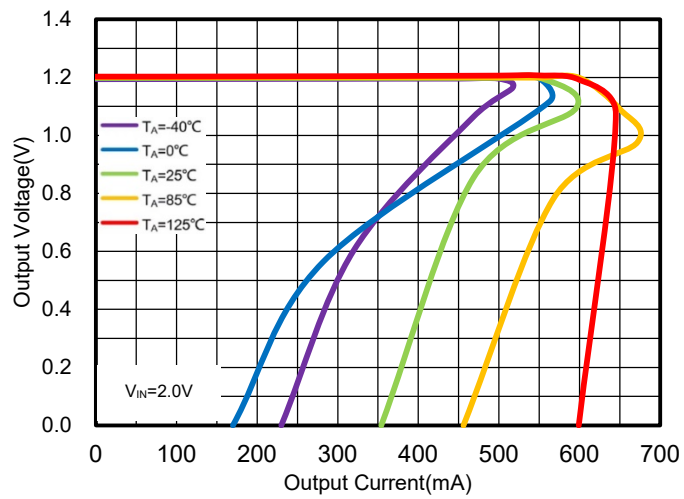


Figure 29. WR0340-12A50R
Foldback Current Limit vs I_{OUT} & Ambient Temperature

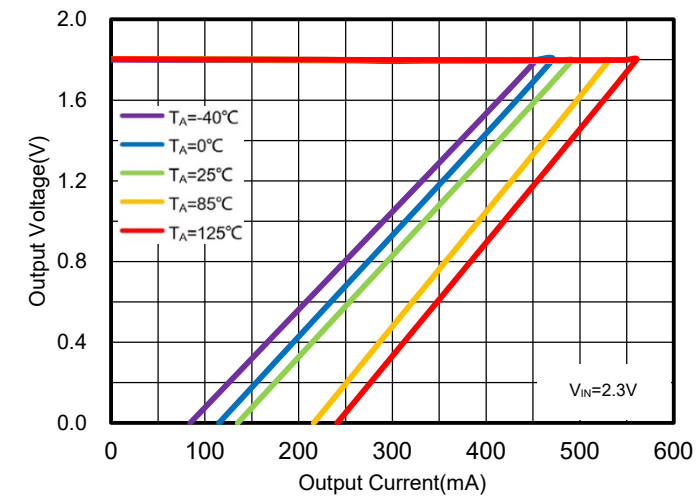


Figure 30. WR0340-18FF4R
Foldback Current Limit vs I_{OUT} & Ambient Temperature

Typical Characteristics(V_{IN} = $V_{OUT\ (NOMINAL)}$ + 0.5 V or 2.0 V (whichever is greater), C_{IN} = C_{OUT} = 1μF, Full= -40℃ to 125℃, unless otherwise noted)

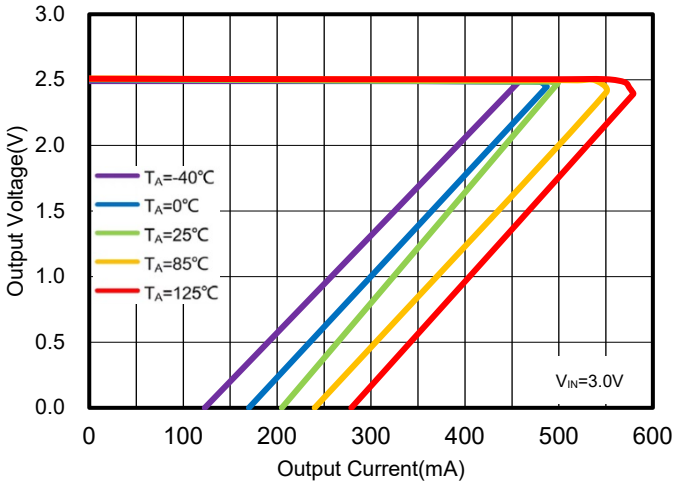


Figure 31. WR0340-25A50R
Foldback Current Limit vs I_{OUT} & Ambient Temperature

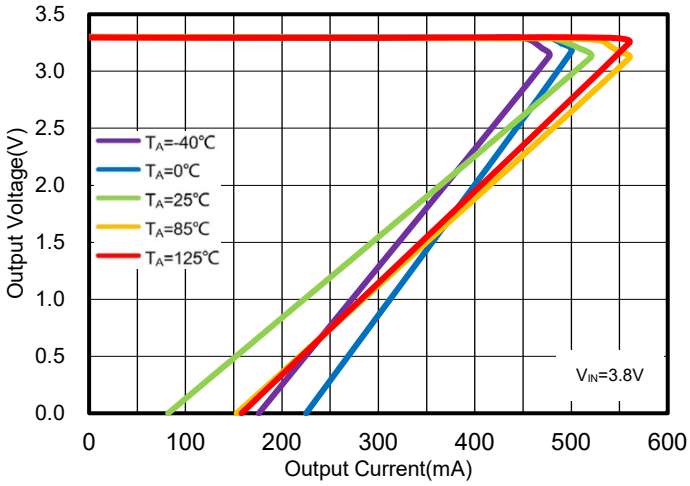


Figure 32. WR0340-33FF4R
Foldback Current Limit vs I_{OUT} & Ambient Temperature

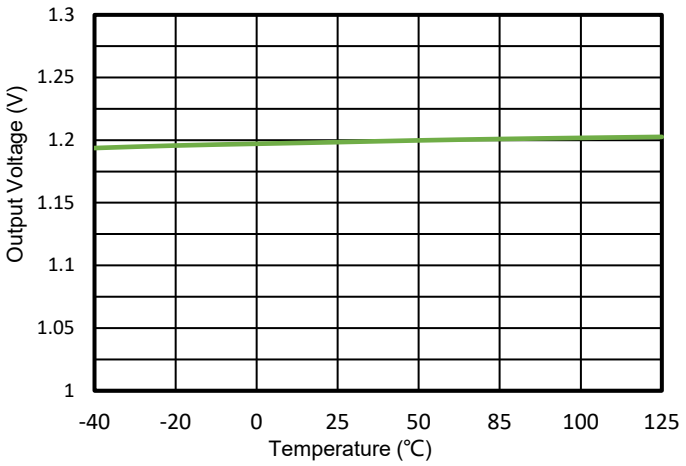


Figure 33. WR0340-12A50R
Output Voltage vs Ambient Temperature

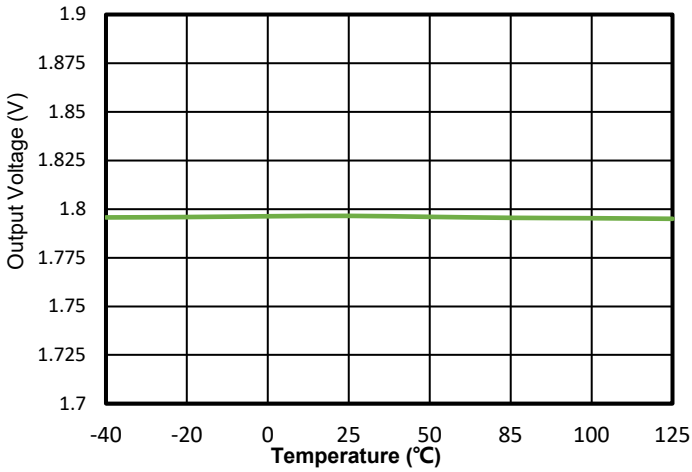


Figure 34. WR0340-18FF4R
Output Voltage vs Ambient Temperature

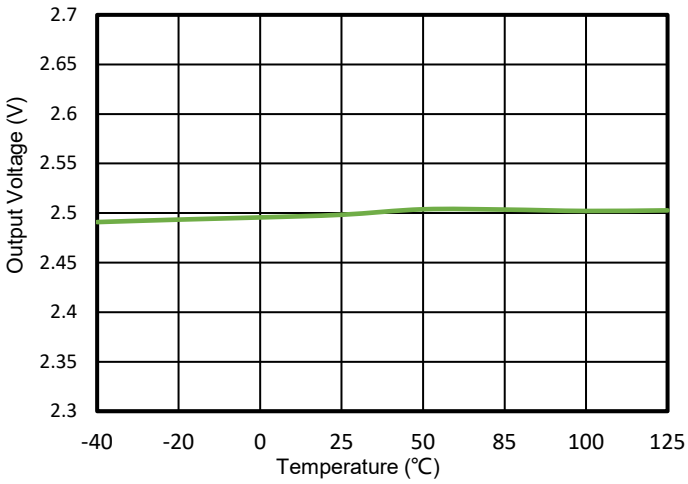


Figure 35. WR0340-25A50R
Output Voltage vs Ambient Temperature

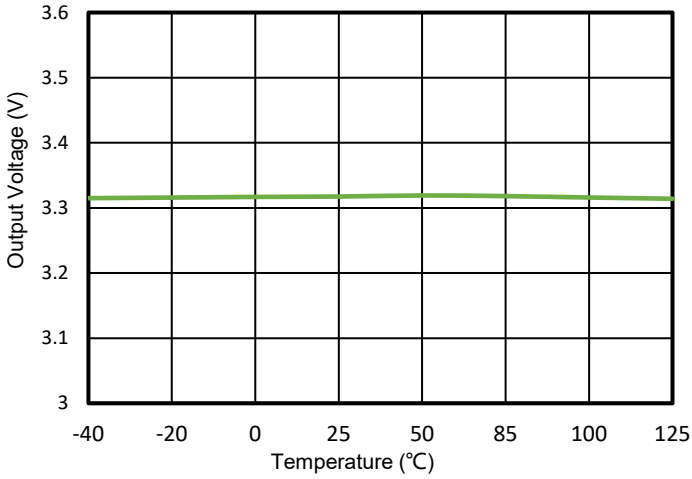


Figure 36. WR0340-33FF4R
Output Voltage vs Ambient Temperature

Typical Characteristics (V_{IN} = $V_{OUT\ (NOMINAL)}$ + 0.5 V or 2.0 V (whichever is greater), C_{IN} = C_{OUT} = 1μF, Full= -40℃ to 125℃, unless otherwise noted)

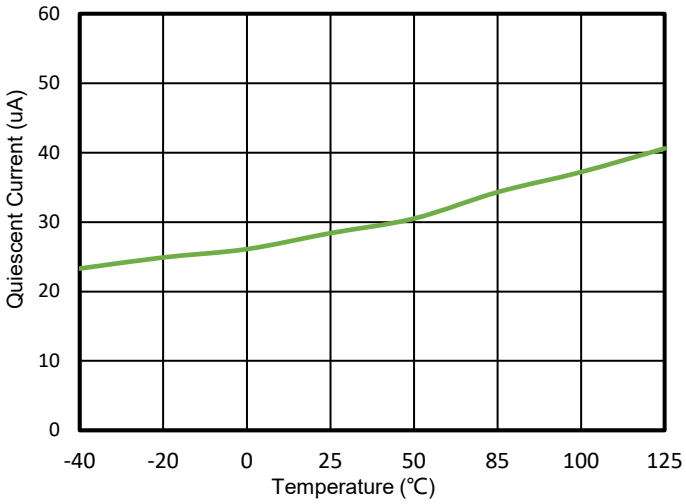


Figure 37. WR0340-12A50R
Quiescent Current vs Ambient Temperature

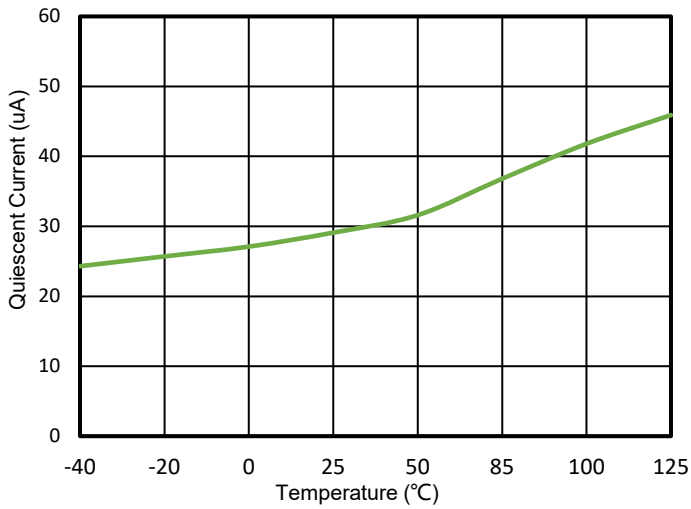


Figure 38. WR0340-18FF4R
Quiescent Current vs Ambient Temperature

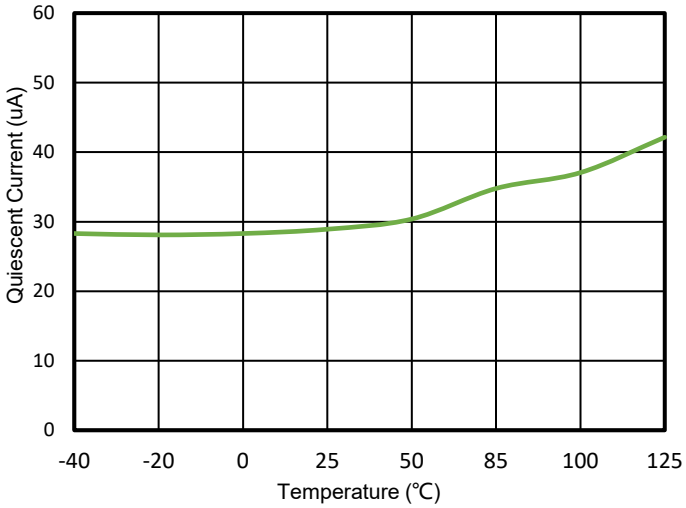


Figure 39. WR0340-25A50R
Quiescent Current vs Ambient Temperature

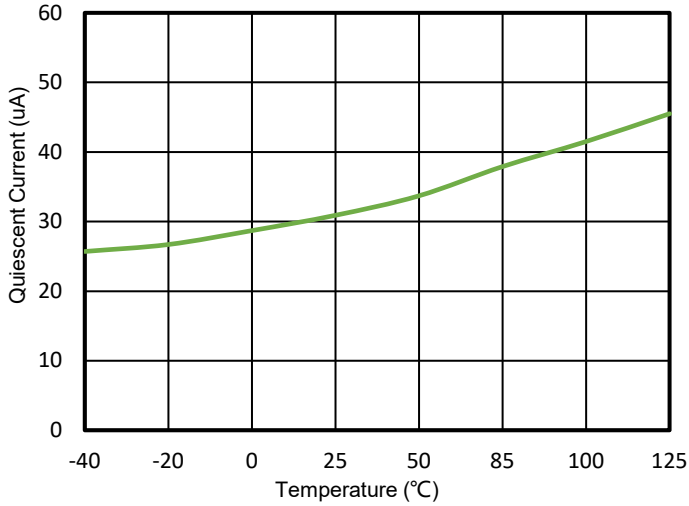


Figure 40. WR0340-33FF4R
Quiescent Current vs Ambient Temperature

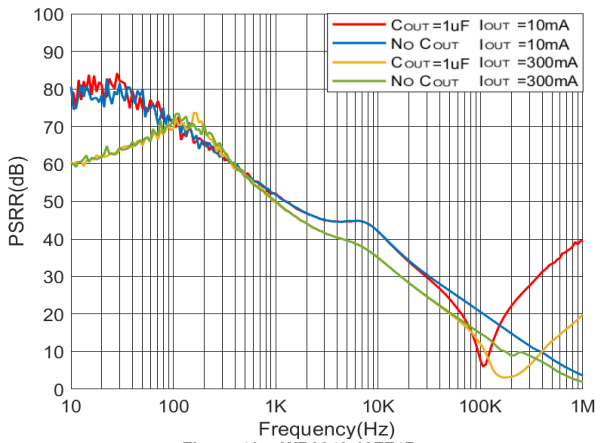


Figure 41. WR0340-18FF4R
Power-Supply Rejection Ratio vs Frequency

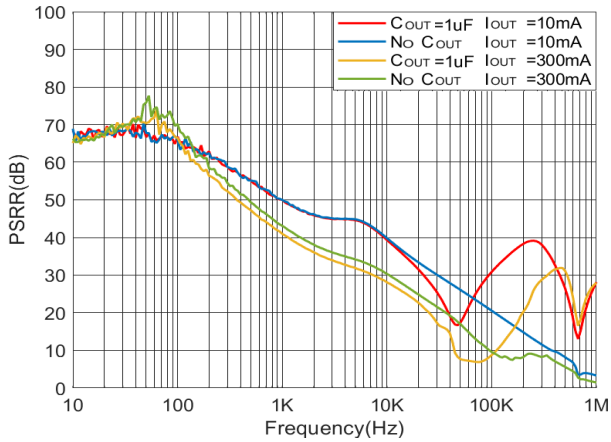


Figure 42. WR0340-25A50R
Power-Supply Rejection Ratio vs Frequency

Typical Characteristics (V_{IN} = $V_{OUT\ (NOMINAL)}$ + 0.5 V or 2.0 V (whichever is greater), C_{IN} = C_{OUT} = 1μF, Full= -40℃ to 125℃, unless otherwise noted)

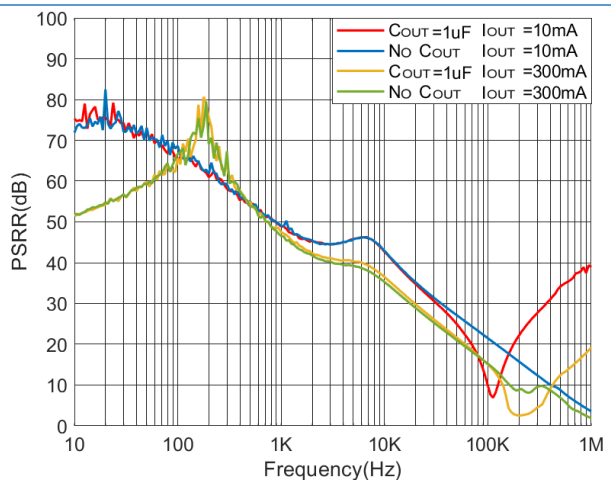


Figure 43. WR0340-33FF4R
Power-Supply Rejection Ratio vs Frequency

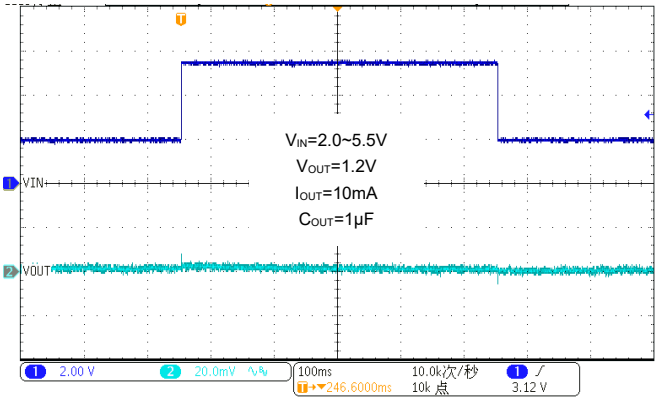


Figure 44. WR0340-12A50R
Line Transient

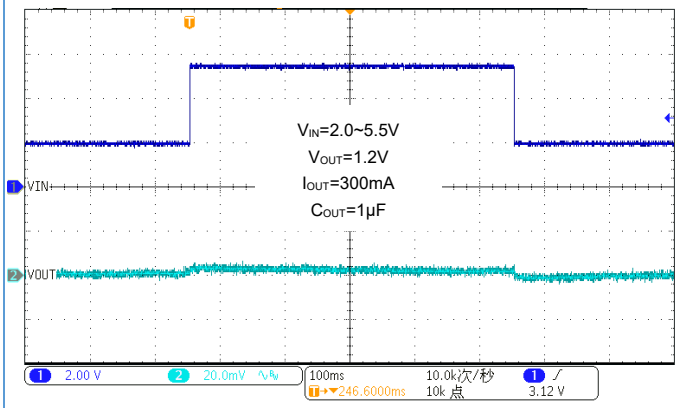


Figure 45. WR0340-12A50R
Line Transient

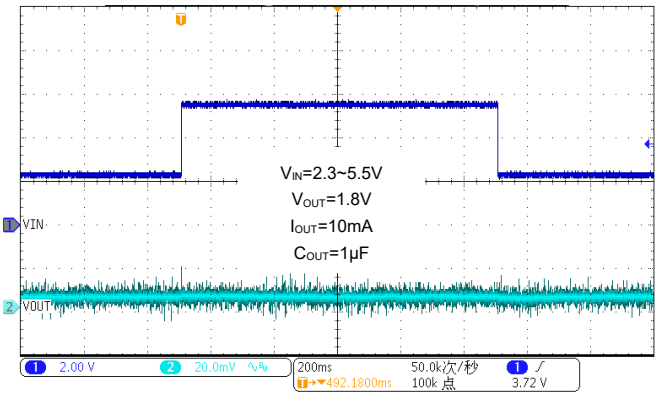


Figure 46. WR0340-18FF4R
Line Transient

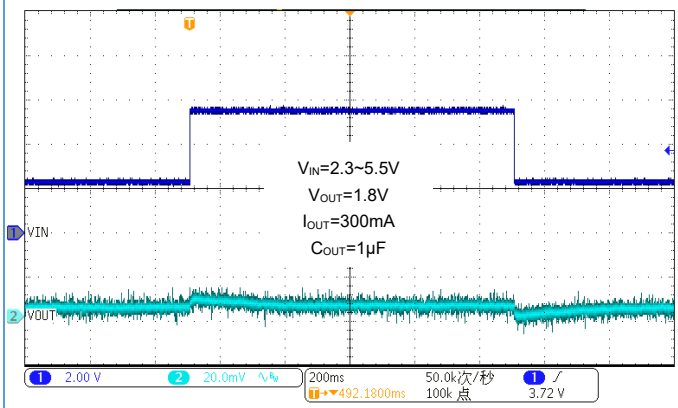


Figure 47. WR0340-18FF4R
Line Transient

Typical Characteristics (V_{IN} = $V_{OUT\ (NOMINAL)}$ + 0.5 V or 2.0 V (whichever is greater), C_{IN} = C_{OUT} = 1μF, Full= -40℃ to 125℃, unless otherwise noted)

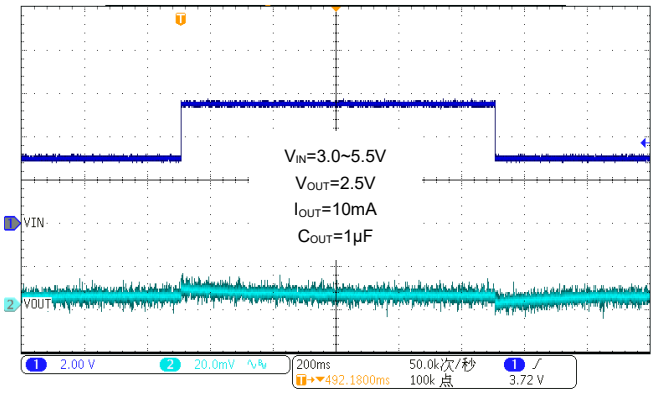


Figure 48. WR0340-25A50R Line Transient

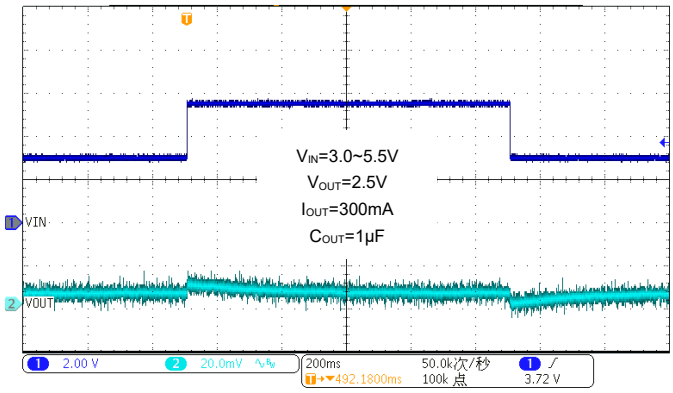


Figure 49. WR0340-25A50R Line Transient

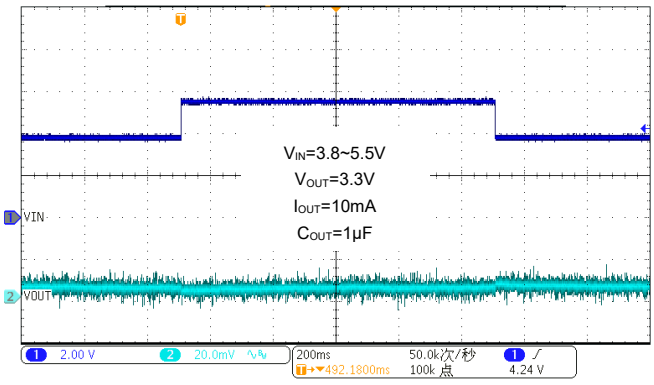


Figure 50. WR0340-33FF4R Line Transient

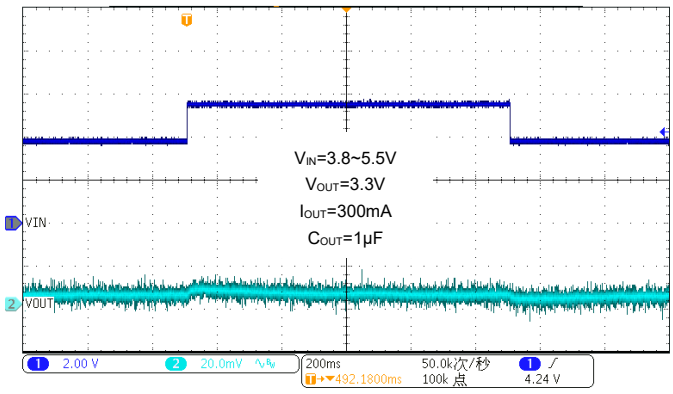


Figure 51. WR0340-33FF4R Line Transient

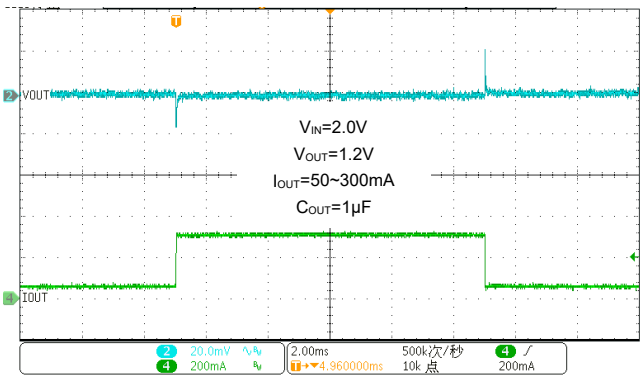


Figure 52. WR0340-12A50R 50mA to 300mA Load Transient

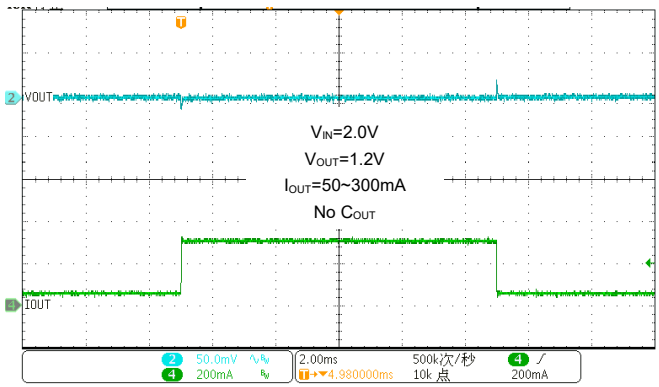


Figure 53. WR0340-12A50R 50mA to 300mA Load Transient

Typical Characteristics (V_{IN} = $V_{OUT\ (NOMINAL)}$ + 0.5 V or 2.0 V (whichever is greater), C_{IN} = C_{OUT} = 1μF, Full= -40℃ to 125℃, unless otherwise noted)

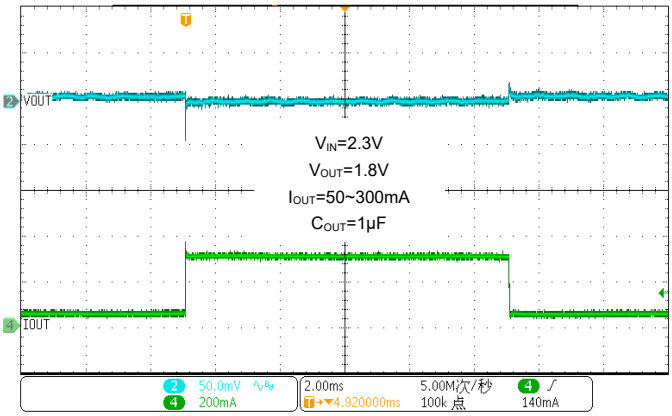


Figure 54. WR0340-18FF4R
50mA to 300mA Load Transient

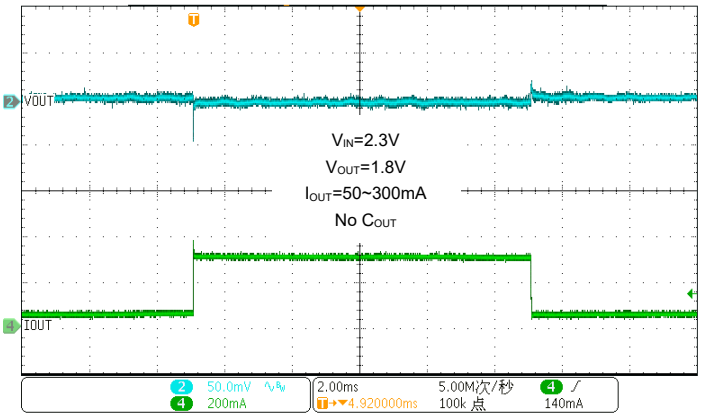


Figure 55. WR0340-18FF4R
50mA to 300mA Load Transient

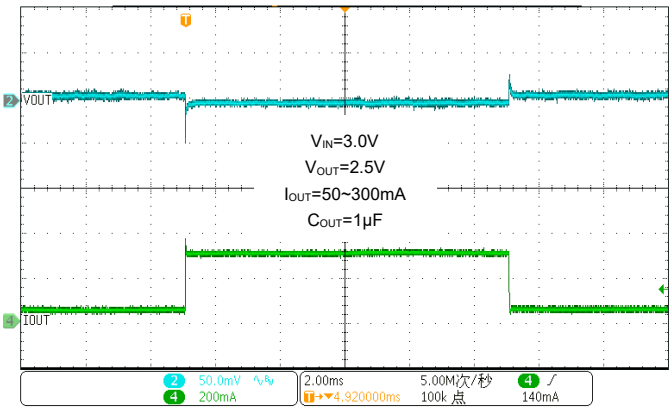


Figure 56. WR0340-25A50R
50mA to 300mA Load Transient

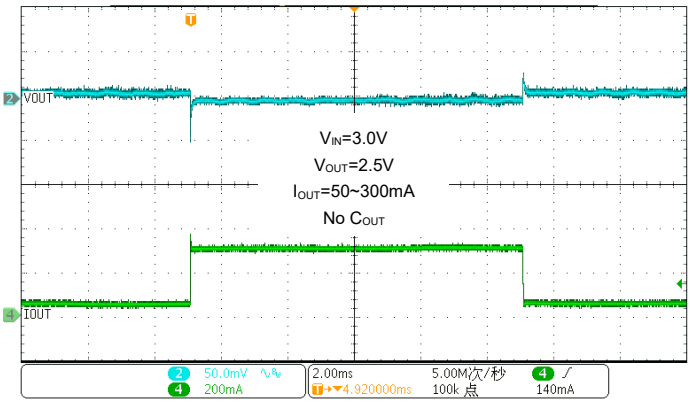


Figure 57. WR0340-25A50R
50mA to 300mA Load Transient

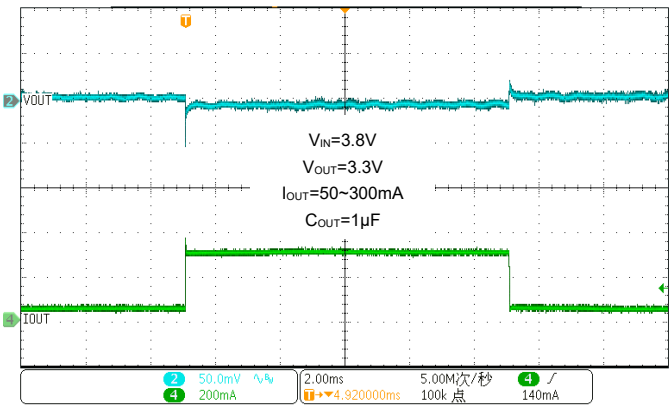


Figure 58. WR0340-33FF4R
50mA to 300mA Load Transient

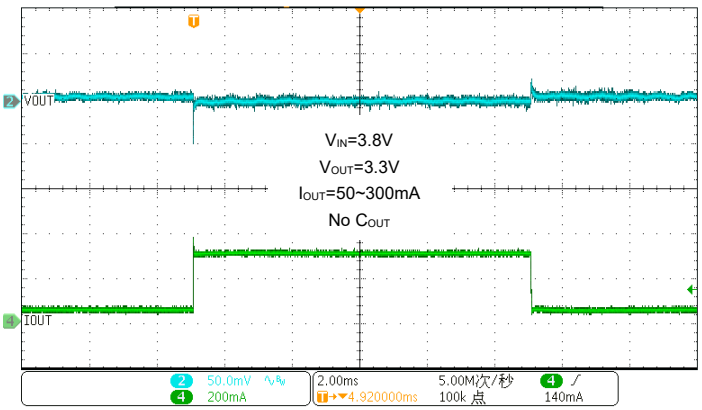


Figure 59. WR0340-33FF4R
50mA to 300mA Load Transient

Typical Characteristics(V_{IN} = $V_{OUT\ (NOMINAL)}$ + 0.5 V or 2.0 V (whichever is greater), C_{IN} = C_{OUT} = 1μF, Full= -40℃ to 125℃, unless otherwise noted)

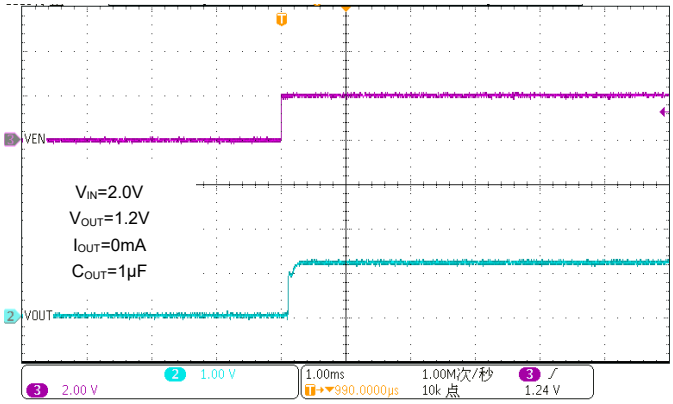


Figure 60. WR0340-12A50R
Startup with EN

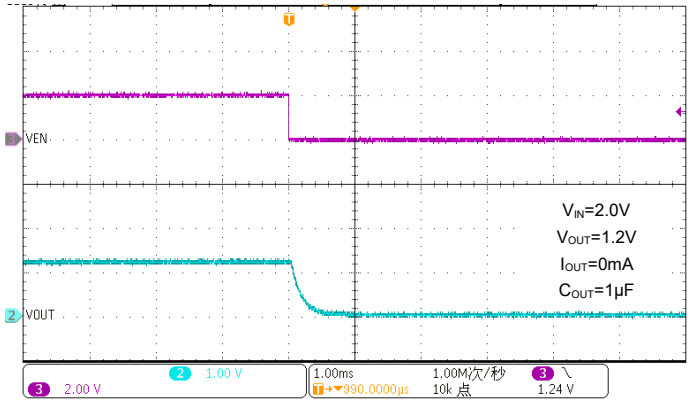


Figure 61. WR0340-12A50R
Shutdown Response with Enable

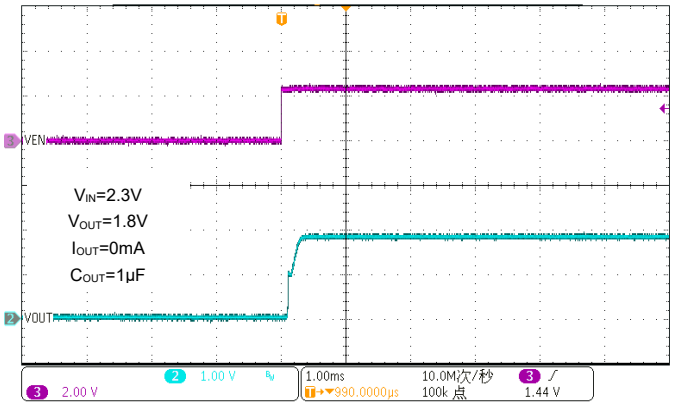


Figure 62. WR0340-18FF4R
Startup with EN

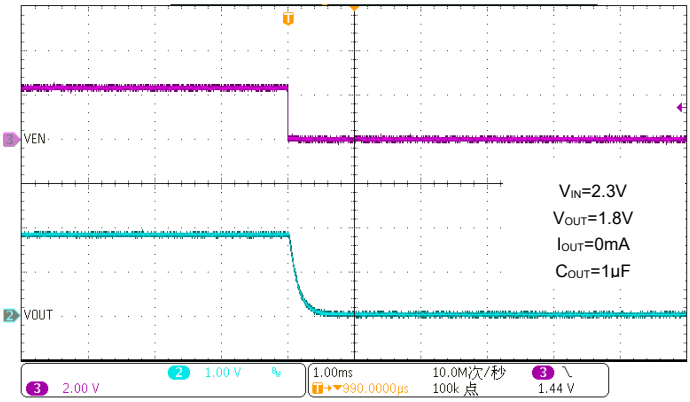


Figure 63. WR0340-18FF4R
Shutdown Response with Enable

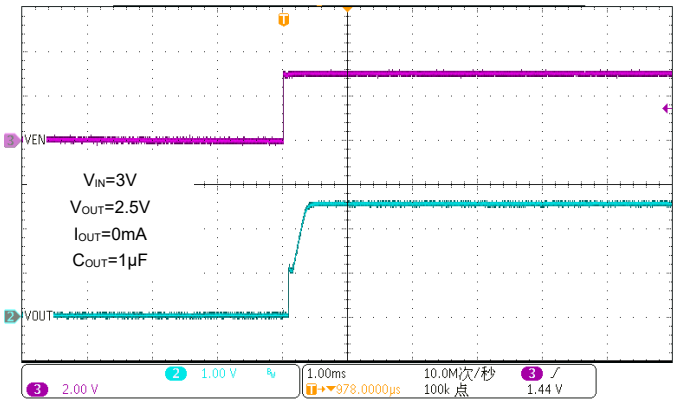


Figure 64. WR0340-25A50R
Startup with EN

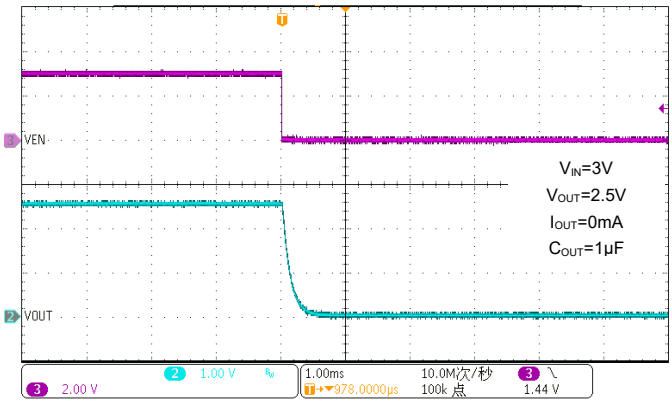


Figure 65. WR0340-25A50R
Shutdown Response with Enable

Typical Characteristics (V_{IN} = $V_{OUT\ (NOMINAL)}$ + 0.5 V or 2.0 V (whichever is greater), C_{IN} = C_{OUT} = 1μF, Full= -40℃ to 125℃, unless otherwise noted)

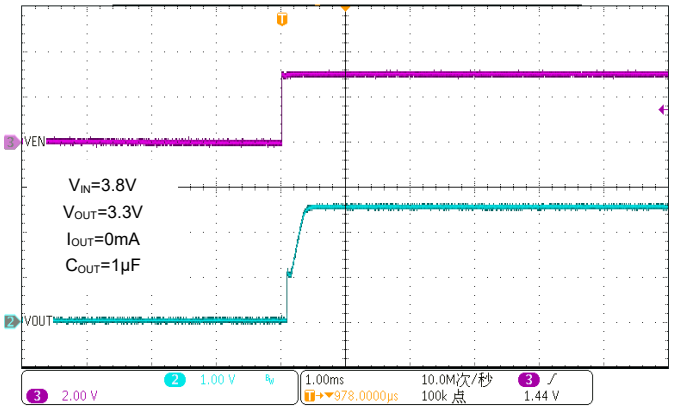


Figure 66. WR0340-33FF4R
Startup with EN

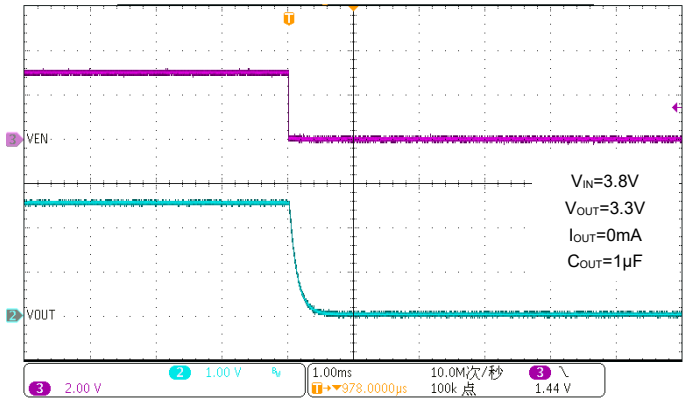


Figure 67. WR0340-33FF4R
Shutdown Response with Enable

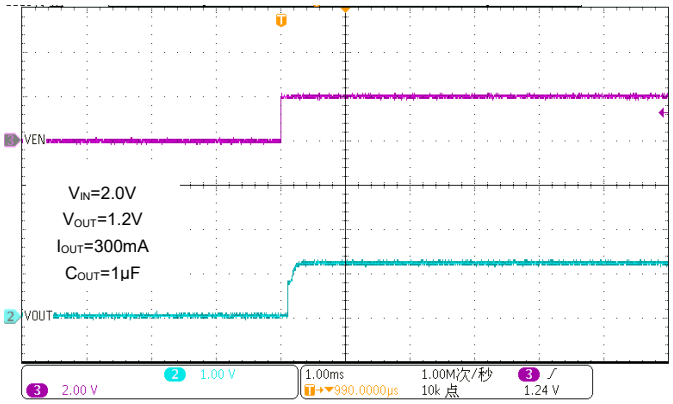


Figure 68. WR0340-12A50R
Startup with EN

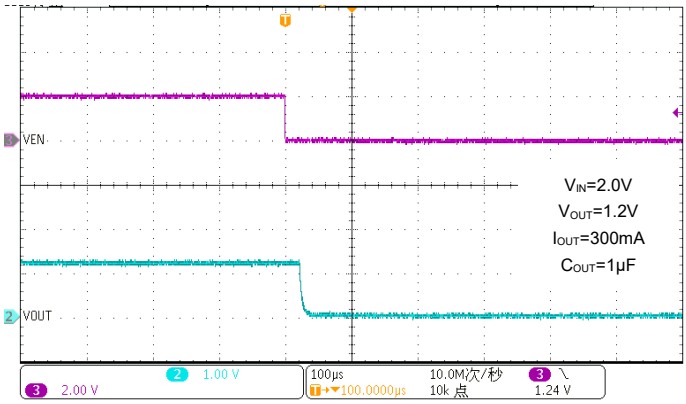


Figure 69. WR0340-12A50R
Shutdown Response with Enable

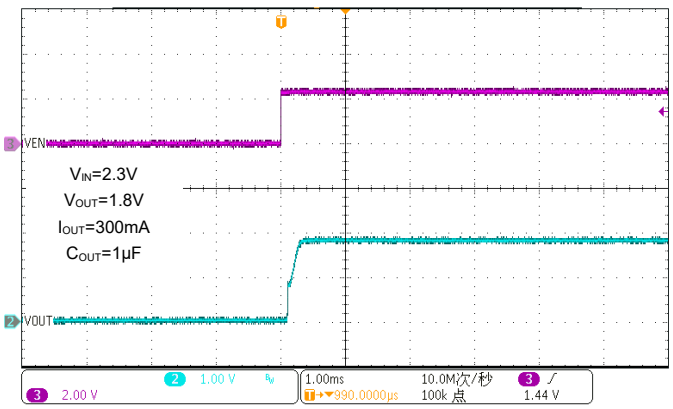


Figure 70. WR0340-18FF4R
Startup with EN

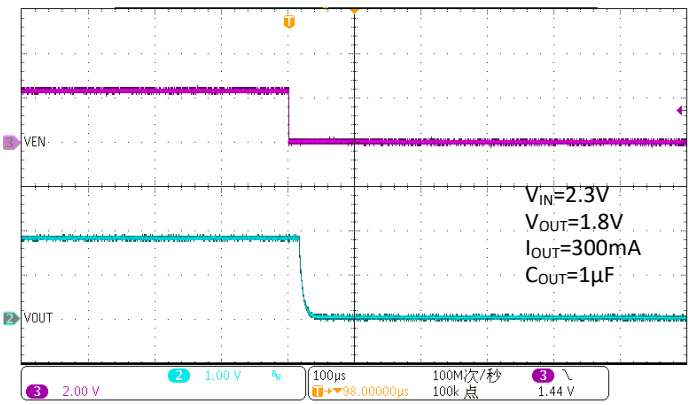


Figure 71. WR0340-18FF4R
Shutdown Response with Enable

Typical Characteristics (V_{IN} = $V_{OUT\ (NOMINAL)}$ + 0.5 V or 2.0 V (whichever is greater), C_{IN} = C_{OUT} = 1μF, Full= -40℃ to 125℃, unless otherwise noted)

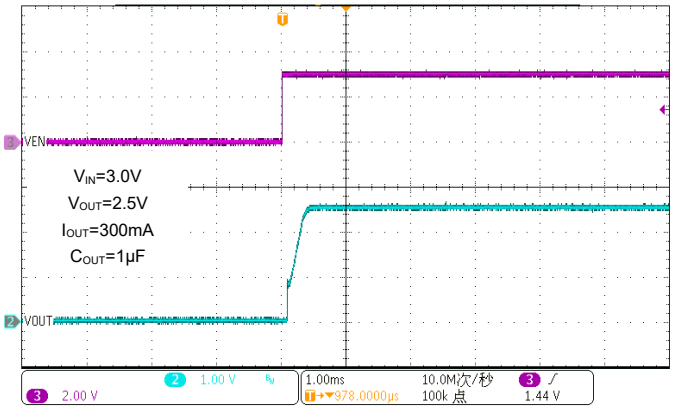


Figure 72. WR0340-25A50R
Startup with EN

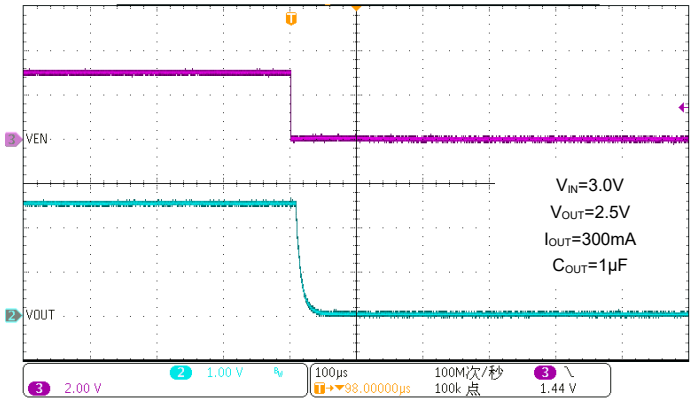


Figure 73. WR0340-25A50R
Shutdown Response with Enable

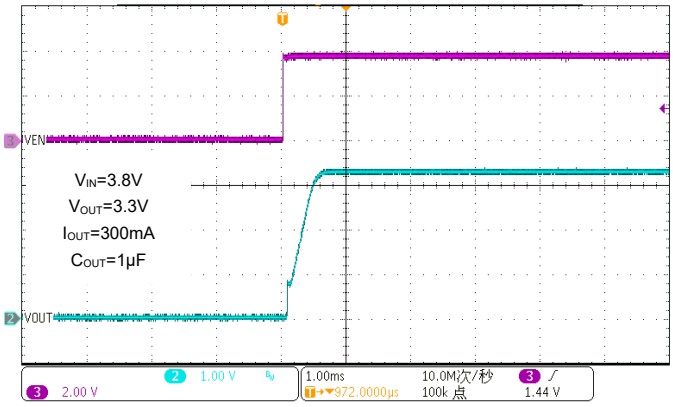


Figure 74. WR0340-33FF4R
Startup with EN

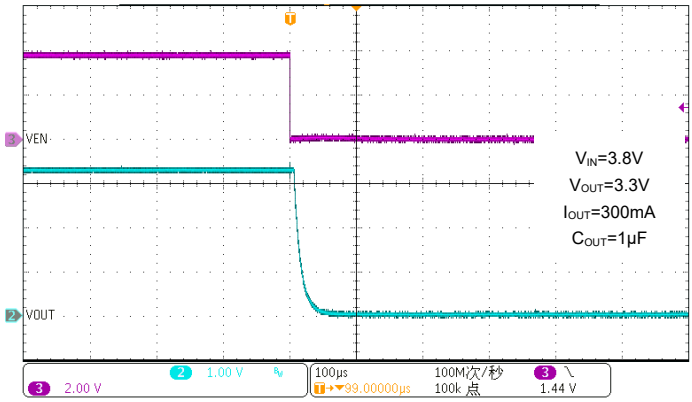


Figure 75. WR0340-33FF4R
Shutdown Response with Enable

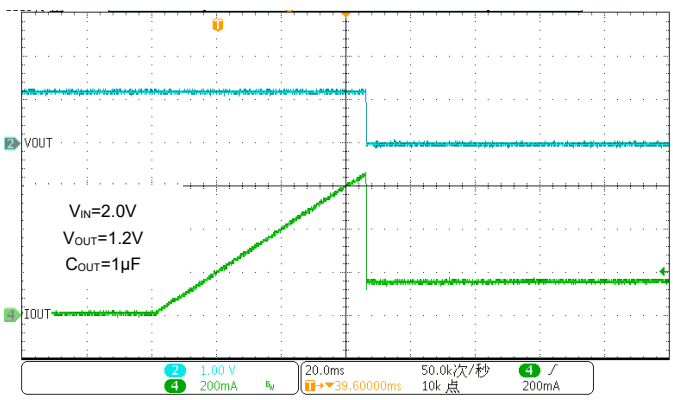


Figure 76. WR0340-12A50R
Foldback Current Limit Response

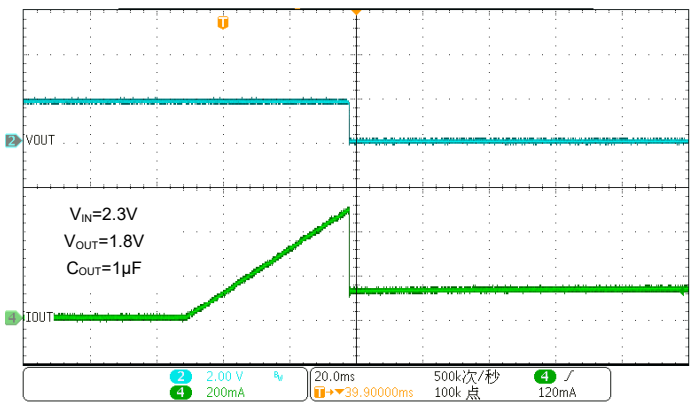


Figure 77. WR0340-18FF4R
Foldback Current Limit Response

Typical Characteristics (V_{IN} = $V_{OUT\ (NOMINAL)}$ + 0.5 V or 2.0 V (whichever is greater), C_{IN} = C_{OUT} = 1μF, Full= -40℃ to 125℃, unless otherwise noted)

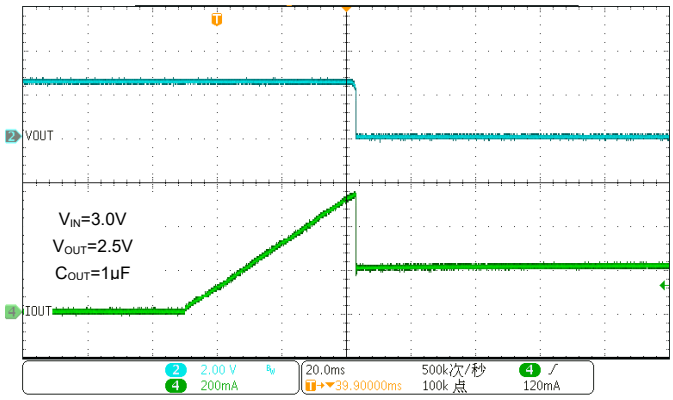


Figure 78. WR0340-25A50R
Foldback Current Limit Response

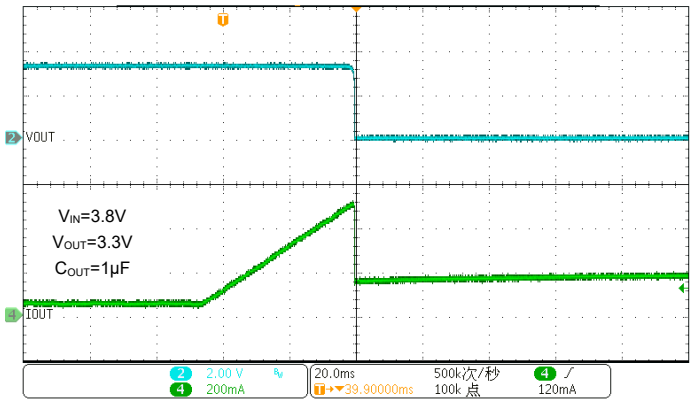


Figure 79. WR0340-33FF4R
Foldback Current Limit Response

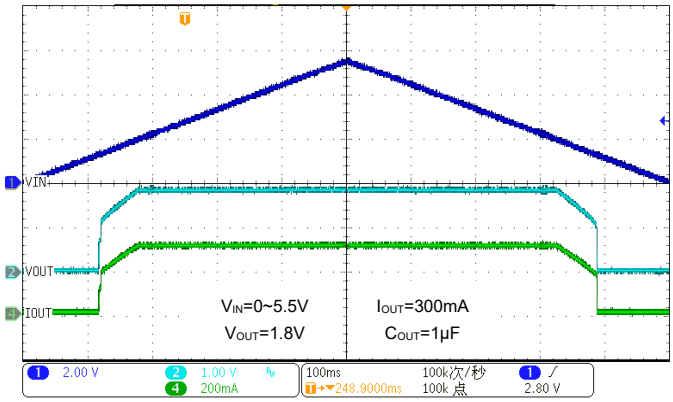


Figure 80. WR0340-18FF4R
V_{IN} Power-Up & Power-Down

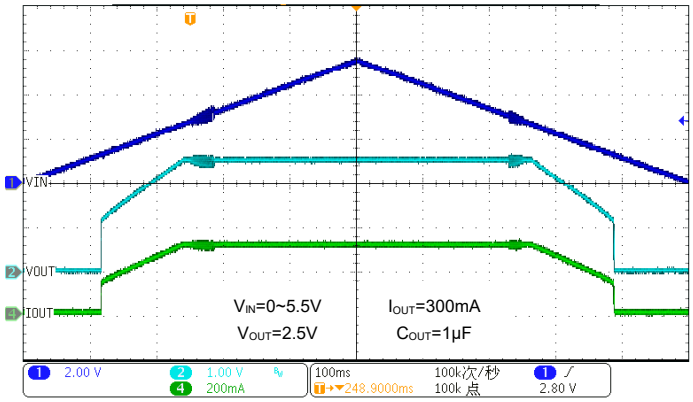


Figure 81. WR0340-25A50R
V_{IN} Power-Up & Power-Down

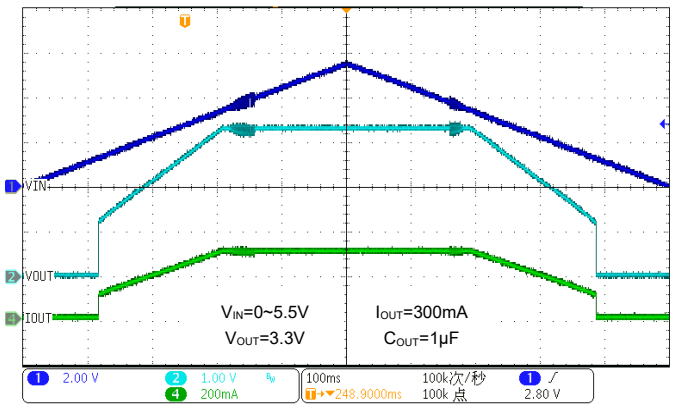


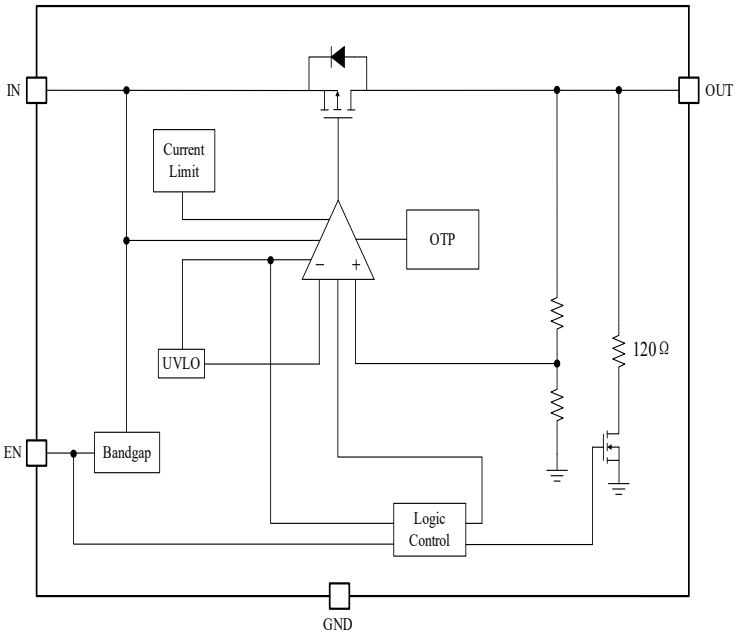
Figure 82. WR0340-33FF4R
V_{IN} Power-Up & Power-Down

11. Function Description

11.1 Overview

The WR0340 series are CMOS-based low-dropout, low-quiescent current linear regulators, offering 300mA with low dropout voltage and high output accuracy. The WR0340 series is designed with a capacitor-free architecture to ensure stability without an input or output capacitor. The device also offers low quiescent current, low-dropout voltage and very small packages suitable for space constrains application.

11.2 Block Diagram



11.3 Feature Description

11.3.1 Output Voltage Accuracy

The WR0340 has an output voltage accuracy of 2%. Output voltage accuracy is defined as the maximum and minimum error in output voltage. This includes the errors introduced by internal reference, load regulation and line regulation differences over the full range of rated load and line operating conditions, taking into account differences between manufacturing lots.

11.3.2 Enable (EN)

The enable pin of WR0340 can control the turn-on and turn-off of the chip. When the input voltage of the enable pin is higher than the high enable voltage threshold, the device outputs normally. When the input voltage of the enable pin is lower than the low input voltage threshold of the EN pin, the device outputs normally. If you do not need to control the output voltage independently, connect the enable pin to the input of the device.

11.3.3 Undervoltage Lockout (UVLO)

When V_{IN} is less than the UVLO threshold, the WR0340 disables the output using an undervoltage lockout (UVLO) circuit, which ensures that the device does not exhibit any unpredictable behavior until the input voltage is greater than the UVLO threshold voltage. During UVLO disabled, the output is pulled to ground through a 120Ω pulldown resistor.

11.3.4 Dropout Voltage (V_{DO})

WR0340 is a low dropout voltage LDO that can achieve nominal output voltage at lower input voltages. Dropout voltage is defined as the value of V_{IN}-V_{OUT} within the output voltage accuracy range when the output current is the maximum rated output current. When the input voltage is below the nominal output voltage, the output voltage varies with the input voltage. For CMOS regulators, the dropout voltage is determined by the $R_{DS\ (ON)}$ of the pass-FET.

The $R_{DS\ (ON)}$ is calculated as follows:

$$R_{DS\ (ON)}=V_{DO}/I_{RATED}$$

11.3.5 Power Supply Rejection Ratio(PSRR)

PSRR, which stands for Power Supply Rejection Ratio, represents the ratio of the two voltage gains obtained when the input and output power supplies are considered as two independent sources.

The basic calculation formula is

$$\mathbf{PSRR = 20log(Ripple(in) / Ripple(out))}$$

The units are in decibels (dB) and the logarithmic ratio is used.

The above equation shows that the output signal is influenced by the power supply in general, in addition to the circuit itself. PSRR is a quantity used to describe how the output signal is affected by the power supply; the larger the PSRR, the less the output signal is affected by the power supply.

As the level of integration continues to increase, the magnitude of supply current required is also increasing. End users want to extend battery life, i.e. they need very efficient DC/DC conversion processes, using more efficient switching regulators. However, switching regulators generate more ripple in the power line than linear regulators.

The PSRR shows the ability of the LDO to suppress input voltage noise. For a clean, noise-free DC output voltage, use an LDO with a high PSRR.

Noise coupling from the input voltage to the internal reference voltage is the main cause of PSRR performance degradation. Using noise reduction capacitors at the input can effectively filter out noise and improve PSRR performance at low frequencies. The LDO can be used not only to regulate the voltage but also to provide an exceptionally clean DC supply for noise sensitive components.

The WR0340 is a high PSRR LDO that can be used not only for voltage regulation but also for noise cancellation in the power supply.

11.3.6 Noise

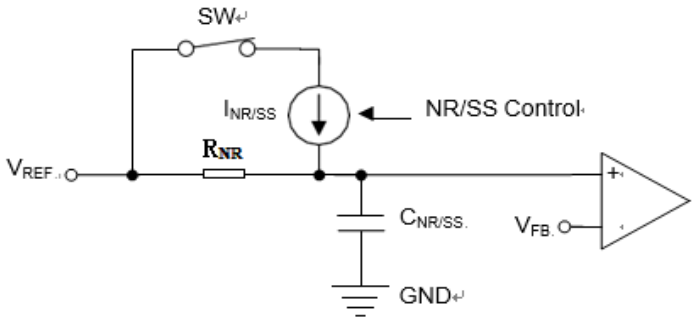
LDO noise can be divided into two main categories: internal noise and external noise. Internal noise is the noise generated inside the electronics; external noise is the noise transmitted from outside the circuit to the circuit. The error amplifier determines the PSRR of the LDO and therefore its ability to suppress external noise at the input; internal noise is always present at the output of the LDO.

In practice, minimising noise from the power supply is critical to system performance. In test and measurement systems, small fluctuations in power supply noise can alter the instantaneous measurement accuracy.

The WR0340 has a low noise reference to ensure that output noise is reduced during normal operation.

11.3.7 Output Soft-Start

Soft-start is the ramping characteristic of the output voltage during the LDO turn-on period after EN and UVLO have exceeded the threshold, preventing the damage caused by output voltage overshoot to the subordinate circuits and enabling effective protection of the secondary circuits. The soft-start ramp can be programmed using a noise reduction capacitor ($C_{NR/SS}$). A larger value of noise reduction capacitor will reduce noise, but will also result in a slower output turn-on ramp. Higher currents allow a reasonable start-up time to be maintained with a larger noise reduction capacitor.



Soft-Start Circuit

11.3.8 Foldback Current Limit (ICL)

In LDO circuits, if an output short circuit or excessive load current occurs, the device may be burned out. Especially in the case of a short circuit, not only is there too much current flowing through the regulator, but the voltage across the source drain of the regulator is also at its maximum, which is likely to burn out the regulator and make the device inoperable. The current limiting circuit used in LDO is a constant current limiting circuit, where the maximum load current that the LDO can supply is limited to a set constant I_{MAX}, and when an overload or short circuit occurs, the output current will be maintained at I_{MAX}, and the output voltage will be reduced to $I_{MAX}R_{LOAD}$.

However, if the external overload or short circuit condition lasts for a long time, the continuous high current will increase the device temperature and increase the power consumption of the whole system. To improve this situation, a foldback current limiting circuit can be used. In a foldback current limiting circuit, both the output current and the output voltage are gradually reduced when the output current reaches the set maximum current I_{MAX}. The output current is reduced to the set current threshold I_{FB} and the output voltage is reduced to $I_{FB}R_{LOAD}$. The output current is clamped to a smaller value in the event of an overload or short circuit and the system power consumption is reduced and the device temperature does not rise significantly.

The foldback current limiting circuit is essentially a constant current limiting circuit with an output voltage feedback loop, so that in the event of an overload or short circuit, the output current is gradually reduced due to the reduction in output voltage and eventually clamped at a smaller value.

The WR0340 uses a foldback current limiting mode where the final current is clamped to around 280mA, thus providing good protection to the device.

More information on current limiting can be found in Electrical Characteristics *Figure 76* to *Figure 79*.

11.3.9 Thermal Protection

The WR0340 contains a thermal shutdown protection circuit that implements the required switching gate circuit function through a thermal switch integrated inside the chip. The output current is turned off when the heat in the LDO is too high. Thermal shutdown occurs when the thermal junction temperature (T_J) of the energized crystal exceeds 160°C (typical). The thermal shutdown hysteresis ensures that the LDO resets (turns on) again when the temperature drops to 135°C (typical). The thermal time constant of the semiconductor chip is quite short, so when thermal shutdown is reached, the output turns on and off at a higher rate until the power dissipation is reduced.

The WR0340's internal protection circuitry is designed to prevent thermal overload conditions. This circuitry is not a substitute for a proper heat sink. Continuously putting the WR0340 into a thermal shutdown state will reduce the reliability of the device.

For reliable operation, limit the ambient temperature to a maximum of 125°C. The thermal margin in a given layout is to be estimated. For good reliability, thermal shutdown must occur at least 35°C above the maximum expected ambient temperature condition of the application.

11.4 Functional Mode Of The Device

The device has three modes: normal, dropout, and disabled modes of operation.

The operating conditions of each mode are listed in the table below.

Operating conditions of each mode

FUNCTIONAL MODE	CONDITIONS			
	V_{IN}	V_{EN}	I_{OUT}	T_J
Normal	$5.5V > V_{IN} > V_{OUT(nom)} + V_{DO}$	$V_{EN} > V_{IH(EN)}$	$I_{OUT} < I_{CL}$	$T_J < T_{sd}$
Dropout	$V_{UVLO} < V_{IN} < V_{OUT(nom)} + V_{DO}$	$V_{EN} > V_{IH(EN)}$	$I_{OUT} < I_{CL}$	$T_J < T_{sd}$
Disabled	$V_{IN} < V_{UVLO}$	$V_{EN} < V_{IL(EN)}$	—	$T_J > T_{sd}$

11.4.1 Normal Mode

Normal operating mode requires that both of the following conditions are met.

1. The input voltage is greater than the rated output voltage plus the differential voltage ($V_{OUT(nom)}$ + V_{DO}) and is less than 5.5V.

2. The enable voltage has previously exceeded the enable rise threshold voltage and has not fallen below the enable fall threshold.

3. The output current is less than the current limit ($I_{OUT} < I_{CL}$).

4. The device junction temperature is less than the thermal shutdown temperature ($T_J < T_{sd}$).

11.4.2 Dropout Mode

If the input voltage is below the rated output voltage plus a specified dropout voltage, but all other conditions are met for normal operation, the device operates in the dropout state and the output voltage tracks the input voltage. Because the transient performance of the device is significantly reduced through the device being in the triode state, the output current is no longer controlled. Line or load transients during power down can result in large output voltage deviations.

11.4.3 Disabled

The WR0340 can be turned off by forcing the enable pin low, typically with an enable voltage below 0.4V, at which point the pass device is turned off, internal circuits are shutdown, and the output voltage is actively discharged to ground through an internal resistor from output to ground.

12. Application

Note: The information in the Applications section below is not part of WAY-ON's product specifications and WAY-ON does not guarantee its accuracy or completeness. The customer is responsible for determining the suitability of the component for its intended use and should verify and test its design implementation to confirm system functionality.

12.1 Application Information

The WR0340 is a linear regulator with an input voltage of 1.4 V to 5.5 V, an output voltage of 1.0 V to 3.3 V, and an output voltage accuracy of 1%. The maximum output current is 300 mA. The efficiency of a linear regulator is determined by the ratio of the output voltage to the input voltage, so to achieve high efficiency, the differential voltage (V_{IN}-V_{OUT}) must be as small as possible. This section discusses how to best use the device in practical applications.

12.1.1 Start-Up

12.1.1.1. Enable(EN)

The WR0340 can determine the output of the device through the EN input voltage, EN is higher than the voltage threshold to turn on, in order to prevent the device from turning off when the input voltage drops during the turn-on period, EN has a certain hysteresis. If you want to use the EN control, you need to give a control voltage to the EN side.

12.1.1.2. Automatic Discharge

The WR0340 has an internal pull-down MOSFET that connects a discharge resistor from V_{OUT} to ground to actively release the output voltage when the device is disabled.

12.1.1.3. Soft-Start

Soft start refers to the characteristic that the output voltage rises gradually as the EN voltage jumps from low to high. Reducing the output voltage rise rate reduces the inrush current that charges the output capacitor. The inrush current is the current entering the LDO during startup and consists of the load current, the current charging the output capacitor, and the ground pin current.

The inrush current can be estimated by the following equation :

$$\mathbf{I_{OUT}(t)} = \left(\frac{\mathbf{C_{OUT}\ x\ dV_{OUT}(t)}}{\mathbf{dt}}\right) + \left(\frac{\mathbf{V_{OUT}(t)}}{\mathbf{R_{LOAD}}}\right)$$

The WR0340 controls soft-start through an external capacitor (CNR/SS), which helps to reduce inrush current and reduce load transients on the input power bus, thus solving startup initialization problems that can result when powering FPGAs, DSPs, or other high-current loads.

12.1.2 Capacitor Recommendation

The WR0340 uses an advanced internal control loop for stable operation with or not input and output capacitors. Dynamic performance is improved by using output capacitor and input capacitor. Using input capacitor cancels reactive input sources and improves transient response, input ripple, and PSRR. Good analog design practice is to connect a 0.1μF to 1μF capacitor between IN and GND. An output capacitor of 0.1μF or larger usually provides good dynamic response. These capacitors also have limitations, ceramic capacitors using X7R-, X5R- and COG grade dielectric materials have relatively good capacitance stability over temperature. Place C_{IN} and C_{OUT} as close as possible to the IN pin and OUT pin to minimize trace inductance from the capacitor to the device.

Increasing the input capacitance can reduce the transient input drop during start-up and load current. If the C_{OUT} produces high Q peak effects during transients, using only very large ceramic input capacitors can cause unwanted ringing at the OUT side, which requires well-designed short interconnects to the upstream supply to reduce ringing. Using a tantalum capacitor with an ESR of several hundred milliohms in parallel with the ceramic input capacitor can avoid unwanted ringing. The load step transient response is the output voltage response of the LDO to a step change in load current. A larger output capacitor reduces any voltage dips or spikes that occur during the load step, but at the same time the control loop bandwidth is reduced, which slows the response time.

Because, the LDO cannot consume charge, the control loop must close through the FET when the output load is removed or greatly reduced and wait for any excess charge to be depleted.

12.1.3 Power Dissipation(PD)

The reliability of the circuit requires reasonable consideration of the power dissipation of the device, the location of the circuit on the PCB, and the proper sizing of the thermal plane. The regulator should be surrounded by no other heat generating devices as much as possible. The power dissipation of the regulator depends on the input and output voltage difference and the load conditions.

P_D can be calculated using the following equation:

$$P_D = (V_{IN} - V_{OUT}) \times I_{OUT}$$

Using the proper input voltage minimizes the power dissipation, resulting in greater efficiency.

To obtain the lowest power dissipation, use the minimum input voltage required for normal output voltage.

The maximum power dissipation determines the maximum allowable ambient temperature (T_A) of the device. Power dissipation and junction temperature are typically related to the junction-ambient thermal resistance (θ_{JA}) and ambient air temperature (T_A) of the PCB and package and are calculated as follows

$$T_J = T_A + (\theta_{JA} \times P_D)$$

The thermal resistance (θ_{JA}) depends primarily on the thermal dispersion capability of the PCB design. The total copper area, copper weight, and the location of the plane all affect the thermal dispersion capability, and the PCB and copper laydown area can only be used as a relative measure of the package's thermal performance.

12.1.4 Estimate the temperature of the junction

As recommended by JEDEC, the psi (Ψ) thermal metrics are used to estimate the junction temperature of the LDO in PCB board applications. These metrics are relative estimates of the junction temperature in actual applications. The thermal indicators Ψ_{JT} or Ψ_{JB} are given in the thermal information table and can be used according to the following equation.

$$\Psi_{JT}: T_J = T_T + \Psi_{JT} \times P_D$$

$$\Psi_{JB}: T_J = T_B + \Psi_{JB} \times P_D$$

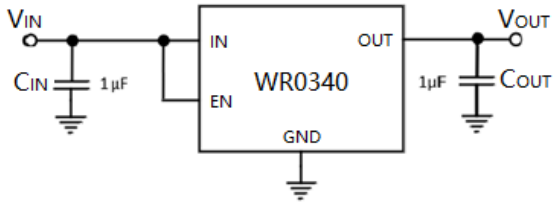
Notes.

- P_D is the power dissipated.
- T_T is the temperature at the top center of the device package.
- T_B is the PCB surface temperature measured 1 mm from the device package and centered on the package.

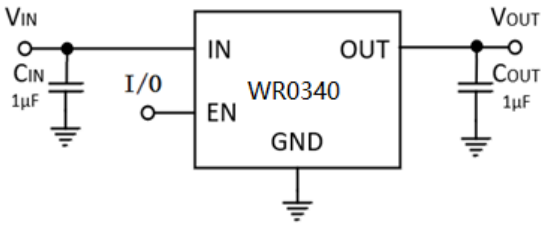
12.2 Typical Application

This section discusses the application of the WR0340 in the circuit. The following figure shows the schematic of the application circuit.

Circuit schematic 1: V_{OUT} normally open, no control.



Circuit schematic 2: V_{OUT} control by external voltage to EN.



Whether or not the WR0340 uses input or output capacitors, stabilization is achieved through the internal control loop. Some applications benefit from the removal of output capacitors. In addition to saving space and cost, the removal of the output capacitor reduces inrush current, in these cases, care should be taken to ensure that the load can withstand the additional output voltage deviation. Typically the slew rate increases, the peak voltage deviation increases significantly. For loads exhibiting fast currents with a slew rate higher than 0.1 A/μs, use an output capacitor. For best performance, the recommended input and output capacitors are 1μF, and the output capacitor cannot exceed a maximum of 100 μF.

13. Power supply recommendation

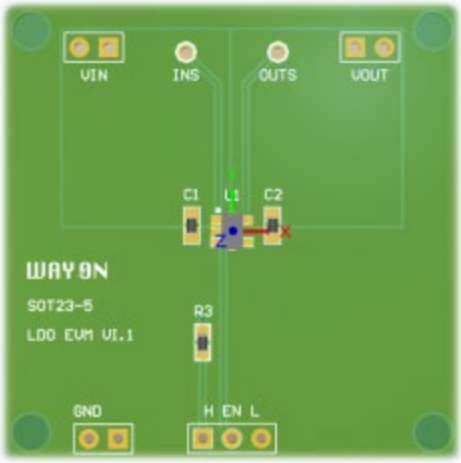
The WR0340 has a V_{IN} range of between 1.4 V and 5.5 V. The input voltage should have some redundancy to ensure a stable output voltage when the load fluctuates. If the input supply is noisy, additional input capacitors can be used to improve the noise performance of the output.

14. Layout Guidelines

The principle of LDO design is to place all components on the same side of the board and connect them as close as possible to their respective LDO pins. Connect the C_{IN} and C_{OUT} grounds, with all LDO ground pins as close together as possible, through a wide copper surface. Using through-holes and long wires for connections is strongly discouraged and can seriously affect system performance.

To improve thermal performance, an array of thermal vias is used to connect the thermal pad to the ground plane. A larger ground plane improves the thermal performance of the device and reduces the operating temperature of the device.

Layout Example：



15. Evaluation Modules

Evaluation Modules (EVMs) are available to help evaluate initial circuit performance. We have evaluation modules for different packages, you can contact us by phone or address at the end to get the evaluation module or schematic.

The module names are listed in the table below.

Name	Package	Evaluation Module
WR0340	SOT23-5	WAYON LDO EVM V1.1 -SOT23-5
	DFN-4	WAYON LDO EVM V1.1 -DFN1*1-4

16. Naming conventions

WR AA BB-CC DDD E

WR: WAYON Regulator

AA: 03 - Output Current, 300mA

BB: Serial number

CC: Output Voltage/AD-Output Voltage, Adjustable Voltage

DDD: A50-Package, SOT23-5

FF4- Package, DFN-4

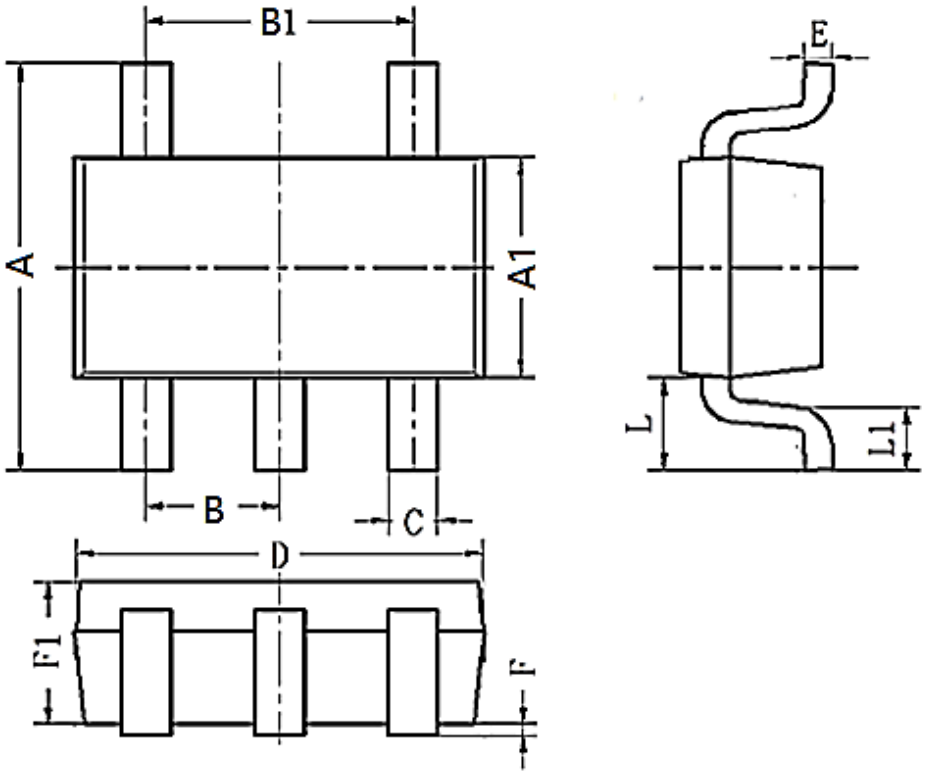
E: R-Reel & T-tube

17. Electrostatic discharge warning

ESD can cause irreversible damage to integrated circuits, ranging from minor performance degradation to device failure. Precision ICs are more susceptible to damage because very minor parameter changes can cause the device to be out of compliance with its published specifications. WAY-ON recommends that all ICs be handled with proper precautions. Failure to follow proper handling practices and installation procedures may damage the IC.

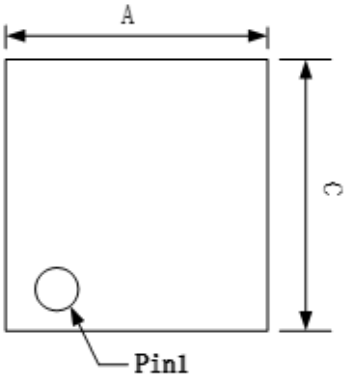
18. Package Information

SOT 23-5

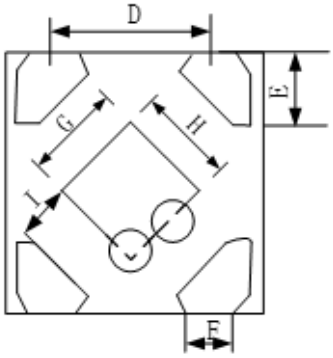


SYMBOL	DIMENSIONS IN MILLIMETERS		
	MIN	NOM	MAX
A	2.60	2.80	3.00
A1	1.50	1.60	1.70
B	0.95BSC		
B1	1.90BSC		
C	0.25	0.40	0.50
D	2.82	2.92	3.02
E	0.10	0.15	0.20
F	0.00	0.08	0.15
L	0.59REF		
F1	0.90	1.10	1.30
L1	0.30	0.45	0.60

DFN-4



Top View



Bottom View

DETAIL A

Pin 1 ID and Tie Bar Mark Options

Note: The configuration of the Pin 1 identifier is optional, but must be located within the zone indicated.

Side View

SYMBOL	DIMENSIONS IN MILLIMETERS		
	MIN	NOM	MAX
A	0.950	1.000	1.050
B	0.320	0.370	0.420
C	0.950	1.000	1.050
D		0.650BSC	
E	0.170	0.270	0.370
F	0.130	0.235	0.300
G	0.430	0.485	0.540
H	0.430	0.485	0.540
I		0.200REF	

19. Ordering Information

Part Number	Output Voltage	Package	Packing Quantity	Marking*
WR0340-10A50R	1.0V	SOT23-5	3k/Reel	WR0340 10 XXXX
WR0340-11A50R	1.1V	SOT23-5	3k/Reel	WR0340 11 XXXX
WR0340-12A50R	1.2V	SOT23-5	3k/Reel	WR0340 12 XXXX
WR0340-15A50R	1.5V	SOT23-5	3k/Reel	WR0340 15 XXXX
WR0340-18A50R	1.8V	SOT23-5	3k/Reel	WR0340 18 XXXX
WR0340-25A50R	2.5V	SOT23-5	3k/Reel	WR0340 25 XXXX
WR0340-28A50R	2.8V	SOT23-5	3k/Reel	WR0340 28 XXXX
WR0340-30A50R	3.0V	SOT23-5	3k/Reel	WR0340 30 XXXX
WR0340-33A50R	3.3V	SOT23-5	3k/Reel	WR0340 33 XXXX
WR0340-10FF4R	1.0V	DFN-4	10k/Reel	340 10
WR0340-11FF4R	1.1V	DFN-4	10k/Reel	340 11
WR0340-12FF4R	1.2V	DFN-4	10k/Reel	340 12
WR0340-15FF4R	1.5V	DFN-4	10k/Reel	340 15
WR0340-18FF4R	1.8V	DFN-4	10k/Reel	340 18
WR0340-25FF4R	2.5V	DFN-4	10k/Reel	340 25
WR0340-28FF4R	2.8V	DFN-4	10k/Reel	340 28
WR0340-30FF4R	3.0V	DFN-4	10k/Reel	340 30
WR0340-33FF4R	3.3V	DFN-4	10k/Reel	340 33

* XXXX is variable.

STATEMENTS

WAY-ON provides data sheets based on the actual performance of the device, and users should verify actual device performance in their specific applications. The device characteristics and parameters in this data sheet can and do vary from application to application, and actual device performance may change over time. This information is intended for developers designing with WAY-ON products. Users are responsible for selecting the appropriate WAY-ON product for their application and for designing and verifying the application to ensure that your application meets the appropriate standards or other requirements, and users are responsible for all consequences. Specifications are subject to change without notice.

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For additional information, please contact your local Sales Representative.