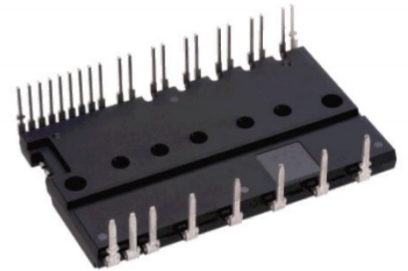


TRM1012BS1 is a 1200V/10A three-phase full bridge intelligent power module with built-in low power loss trench gate field-stop IGBT and FRD, The bootstrap diode BSD is integrated inside, which simplifies PCB design. The internal integrated temperature output VOT function is used to detect the temperature inside the module. The module integrates multiple protection functions, including UVLO under voltage protection and CIN over current protection. The module's input with filtering function and compatible with 3.3V, 5V, and 15V logic input.

MAIN FUNCTION AND RATINGS

- 1200V/10A three-phase full bridge intelligent power module
- Built-in Lower power loss trench gate field-stop IGBT
- Bottom IGBT with emitter output
- Built-in bootstrap diode with current limiting resistor
- VOT linear temperature output
- Compatible with 3.3V, 5V, and 15V logic input
- UVLO under voltage protection, over current protection, over temperature protection

Package: DIP29



APPLICATION

- inverter air-conditioning compressor drive
- Industrial servo converter
- High power inverters' fan and water pump
- Motor driver

PART ORDERING TABLE

Booking information	Product name	Package	Free of Halogen	Packing
TRM1012BS1	TRM1012BS1	DIP29	Yes	Tube

INTERNAL CIRCUIT

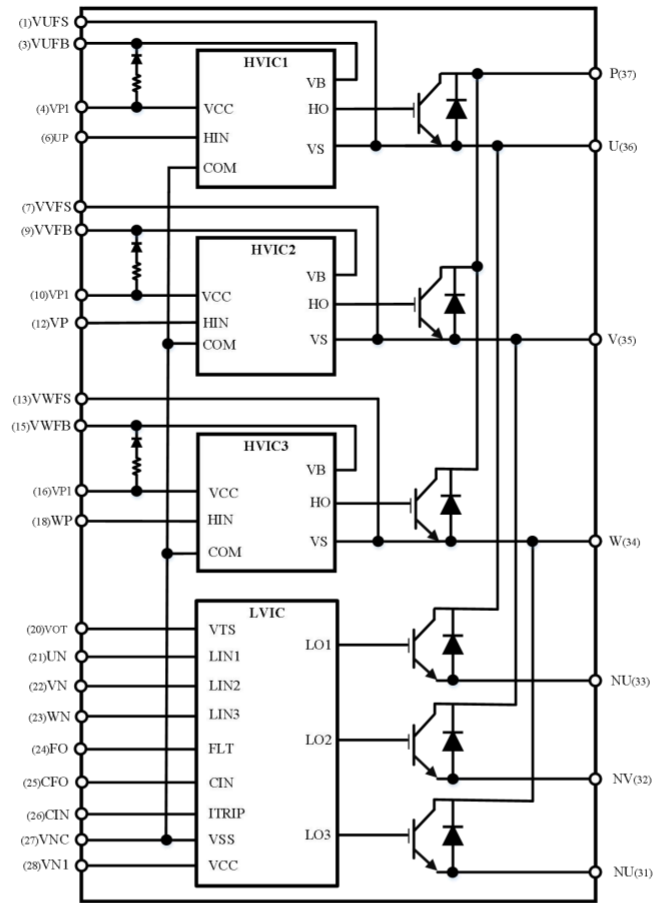


Figure 1 Internal circuit diagram

PIN ASSIGNMENT

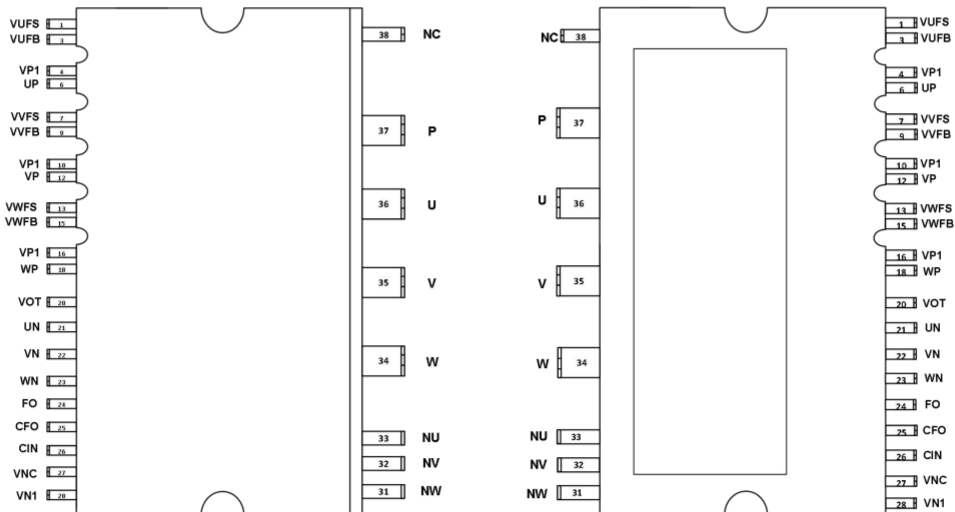


Figure 2 Pin Configuration

PIN DEFINITION

Pin Number	Pin Name	Pin Description
1	VUFS	U-phase upper arm drive ground
3	VUFB	U-phase upper arm drive power supply
4	VP1	U-phase drive power supply
6	UP	U-phase upper arm control signal input
7	VVFS	V-phase upper arm drive ground
9	VVFB	V-phase upper arm drive power supply
10	VP1	V-phase drive power supply
12	VP	V-phase upper arm control signal input
13	VWFS	W-phase upper arm drive ground
15	VWFB	W-phase upper arm drive power supply
16	VP1	W-phase drive power supply
18	WP	W-phase upper arm control signal input
20	VOT	Temperature detection output
21	UN	U-phase lower arm control signal input
22	VN	V-phase lower arm control signal input
23	WN	W-phase lower arm control signal input
24	FO	Fault output
25	CFO	Fault recovery delay input
26	CIN	Over current protection input
27	VNC	Control power supply ground
28	VN1	Control power supply
31	NW	W-phase lower arm IGBT emitter output
32	NV	V-phase lower arm IGBT emitter output
33	NU	U-phase lower arm IGBT emitter output
34	W	W-phase output
35	V	V-phase output
36	U	U-phase output
37	P	Inverter DC input

MAXIMUM RATINGS($T_j = 25^\circ\text{C}$, unless otherwise noted)

INVERTER PART

Symbol	Parameter	Condition	Ratings	Unit
VCC	Supply voltage	Applied between P-NU,NV,NW	900	V
VCC (Surge)	Supply voltage (surge)	Applied between P-NU,NV,NW	1000	
VCES	Collector-emitter voltage		1200	
$\pm I_c$	Each IGBT collector current	$T_c = 25^\circ\text{C}$ (T_c test method Figure 3)	10	A
$\pm I_{cP}$	Each IGBT collector current (peak)	$T_c = 25^\circ\text{C}$, pulse width <1ms	20	
T_j	Junction temperature	(Note 1)	-40~+150	$^\circ\text{C}$

Note 1: The maximum rated junction temperature of the IGBT is 150°C (@ $T_c \leq 100^\circ\text{C}$).To ensure the safe operation of IPM, the junction temperature should be limited to $T_{j(av)} \leq 125^\circ\text{C}$ (@ $T_c \leq 100^\circ\text{C}$).

CONTROL(PROTECTION)PART

Symbol	Parameter	Condition	Ratings	Unit
VDB	P-side control supply voltage	Applied between UFB-U,VFB-V,WFB-W	20	V
VD	Control supply voltage	Applied between VP1-VNC,VN1-VNC	20	
VIN	Input voltage	Applied between UP,VP,WP,UN,VN,WN-VNC	-0.5~VD+0.5	
VFO	Fault output supply voltage	Applied between FO -VNC	-0.5~VD+0.5	
IFO	Fault output current	Sink current at FO terminal	1.5	mA
Vsc	Current sensing input voltage	Applied between CIN-VNC	-0.5~VD+0.5	V

TOTAL SYSTEM

Symbol	Parameter	Condition	Ratings	Unit
VCC(PROT)	Self protection supply voltage limit (Short circuit protection capability)	$V_D = V_{DB} = 13.5-16.5V$, inverter part $T_j = 125^\circ C$, Non-repetitive, less than 2us	800	V
TC	Module case operation temperature	Measurement point of T_c is provided in Figure 3.	-30~+100	$^\circ C$
TSTG	Storage temperature		-40~+125	$^\circ C$
VISO	Isolation voltage	60HZ,Sinusoidal,AC 1min,between connected all pins and heat sink plate	2500	Vrms

T_c MEASUREMENT POINT

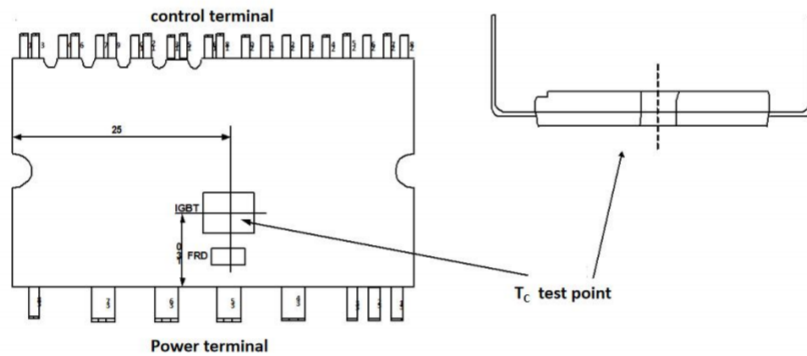


Figure 3 T_c test point

THERMAL RESISTANCE

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
$R_{th(j-c)Q}$	Junction to case thermal resistance	Per IGBT part	-	1.2	-	K/W
$R_{th(j-c)F}$		Per FRD part	-	1.8	-	K/W

ELECTRICAL CHARACTERISTICS: ($T_j = 25^\circ\text{C}$, unless otherwise noted)
INVERTER PART

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
$V_{CE(sat)}$	Collector-emitter saturation voltage	$V_D = V_{DB} = 15\text{V}$ $V_{IN} = 5\text{V}, I_C = 10\text{A},$ $T_j = 25^\circ\text{C}$	-	1.6	2.0	V
		$V_D = V_{DB} = 15\text{V}$ $V_{IN} = 5\text{V}, I_C = 10\text{A},$ $T_j = 150^\circ\text{C}$	-	2.0	-	V
V_{EC}	FWD forward voltage	$V_{IN} = 0\text{V}, I_C = -10\text{A},$ $T_j = 25^\circ\text{C}$	-	2.0	2.4	V
t_{ON}	Switching time (Note 2)	$V_{CC} = 600\text{V},$ $V_D = V_{DB} = 15\text{V}, I_C = 10\text{A}$ $V_{IN} = 0\text{V} \sim 5\text{V},$ inductive loading	500	-	1100	ns
$t_{C(ON)}$			100	-	600	ns
t_{OFF}			1000	-	1600	ns
$t_{C(OFF)}$			200	-	600	ns
t_{rr}			100	-	500	ns
E_{on}	Switching on loss	$I_C = 10\text{A}, V_{CC} = 600\text{V},$	500	-	2000	μJ
E_{off}	Switching off loss	$V_{DB} = V_D = 15\text{V},$ $T_j = 25^\circ\text{C}$	500	-	2000	μJ
I_{CES}	Collector-emitter cut-off current	$V_{CE} = V_{CES} T_j = 25^\circ\text{C}$	-	-	0.1	mA
		$V_{CE} = V_{CES} T_j = 125^\circ\text{C}$	-	-	1	mA

Note 2: t_{ON} and t_{OFF} include the internal transmission delay time of the driver IC. $t_{C(ON)}$ and $t_{C(OFF)}$ are the switching times of the IGBT itself under the internal given gate driving conditions. Please refer to Figure 4 for details.

SWITCHING TIME DEFINITION

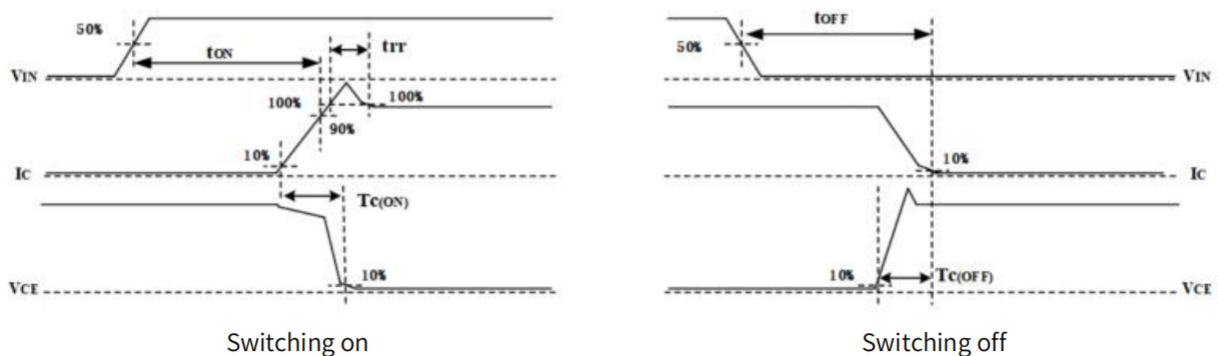


Figure 4 Switching time definition

CONTROL(PROTECTION)PART

Symbol	Parameter	Condition		Min.	Typ.	Max.	Unit
I_D	Circuit current	$V_D = 15V, V_{IN} = 5V$	VP1-VNC	-	3	3.5	mA
I_{DB}		$V_{DB} = 15V, V_{IN} = 5V$	UFB - U, VFB - V, WFB - W	50	-	150	μA
IIN	Input current	$V_{in}=5V$		-	1.0	1.5	mA
V_{FOH}	Fault output voltage	$V_{sc} = 0V$, FO terminal pulled up to 5V by 10K Ω		4.8	-	-	V
V_{FOL}		$V_{sc} = 1V, I_{FO} = 1.5mA$		-	-	0.3	V
$V_{sc,TH+}$	Short circuit trip level	$V_D = 15V$		0.44	0.48	0.52	V
UV_{DD}	Under-voltage protection (UV)	Trip level		-	11	-	V
UV_{DR}		Reset level		-	12	-	
UVDBD		Trip level		-	10.5	-	
UVDBR		Reset level		-	11.5	-	
$R_{on,FLT}$	Fault low effective impedance			-	100	150	ohm
T_{FO}	Fault output pulse width	Without CFO capacitor ($T_{FO} = 10M\Omega \times CFO$)		-	80	-	μs
$T_{FIL,IN}$	Input signal filtering time	$V_{IN} = 0V \& 5V$		-	350	-	ns
T_{CINMIN}	CIN Input signal filtering time	$V_{IN} = 0V \text{ or } 5V, V_{CIN} = 5V$		-	2000	-	ns
VIN(ON)	ON threshold voltage	Applied between UP,VP,WP,UN,VN,WN and VNC		-	-	3.0	V
VIN(OFF)	OFF threshold voltage			0.8	-	-	
V_F	Bootstrap Diode forward voltage	$I_f = 5mA$ including current limiting resistor' s voltage drop (Figure 5)		-	0.7	-	V
RBS	Built-in limiting resistance	Including Bootstrap diode		-	30	-	Ω
VOT	Temperature output	$T_c = 25^\circ C$		-	1.1	-	V
		$T_c = 120^\circ C$		-	3.55	-	

Boost Diode V_F - I_F CURVE

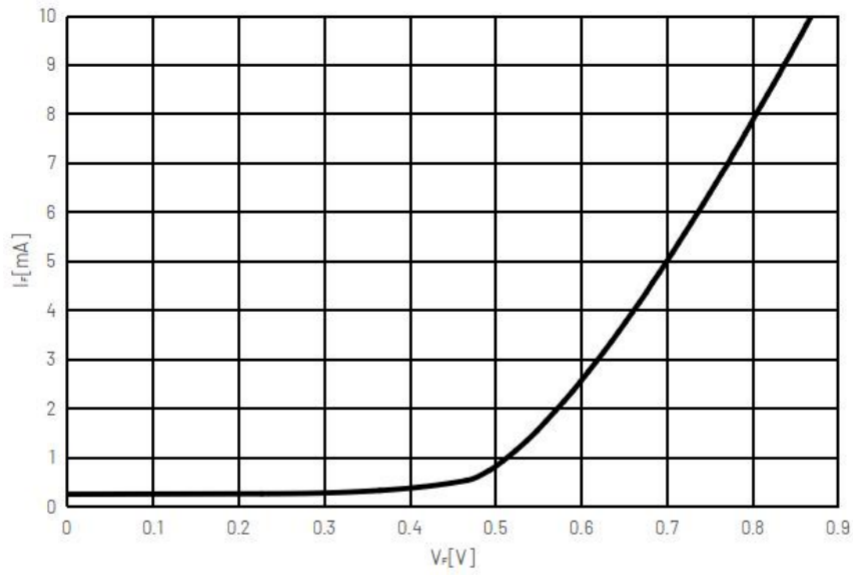
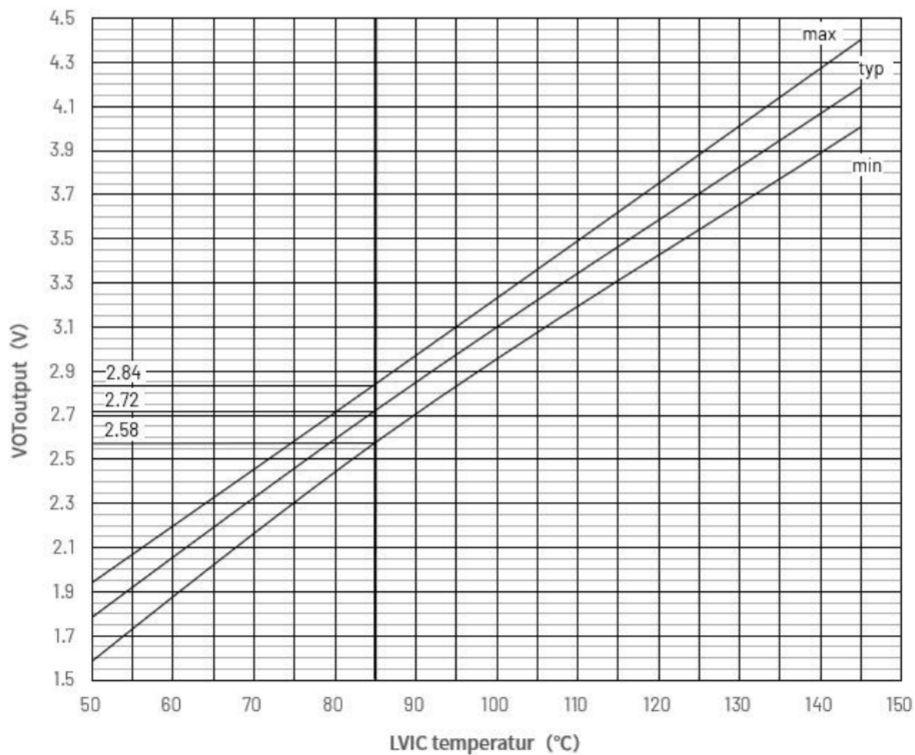


Figure 5 V_F - I_F curve

V_{OT} OUTPUT CURVE



RECOMMENDED OPERATION CONDITIONS

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
V_{cc}	Supply voltage	Applied between P – NU, NV, NW	350	600	800	V
V_D	Control supply voltage	Applied between VP1– VNC	13.5	15	16.5	V
$\Delta V_D, \Delta V_{DB}$	Control voltage variation		-1	-	1	V/ μ s
V_{DB}	Top side supply voltage	Applied between VUFB – U, VVFB – V, VWFB-W .	13	15	18.5	V
T_{dead}	Dead time	For each input signal, $T_c \leq 100^\circ\text{C}$	2	-	-	μ s
f_{PWM}	PWM input frequency	$-20^\circ\text{C} \leq T_c \leq +100^\circ\text{C}$ $-20^\circ\text{C} \leq T_j \leq +150^\circ\text{C}$	-	-	20	kHz
PWM(on)	Minimum input pulse width	ON	1	-	-	μ s
PWM(off)		OFF	2	-	-	μ s
V_{NC}	V_{NC} variation	Between V_{NC} -NU, NV, NW (including surge)	-5.0	-	+5.0	V
T_j	Junction temperature		-20	-	125	$^\circ\text{C}$

MECHANICAL CHARACTERISTICS AND RATINGS

Parameter	Conditions	Min.	Typ.	Max.	Unit
Mounting torque	Mounting screw: M3	-	0.69	-	N·m
Heat-sink flatness	Figure 8	-50	-	+120	μ m
Terminal pulling strength	Control Pin: 4.9N, Power Pin: 9.8N; EIAJ-ED-4701	10	-	-	s

FLATNESS MEASUREMENT

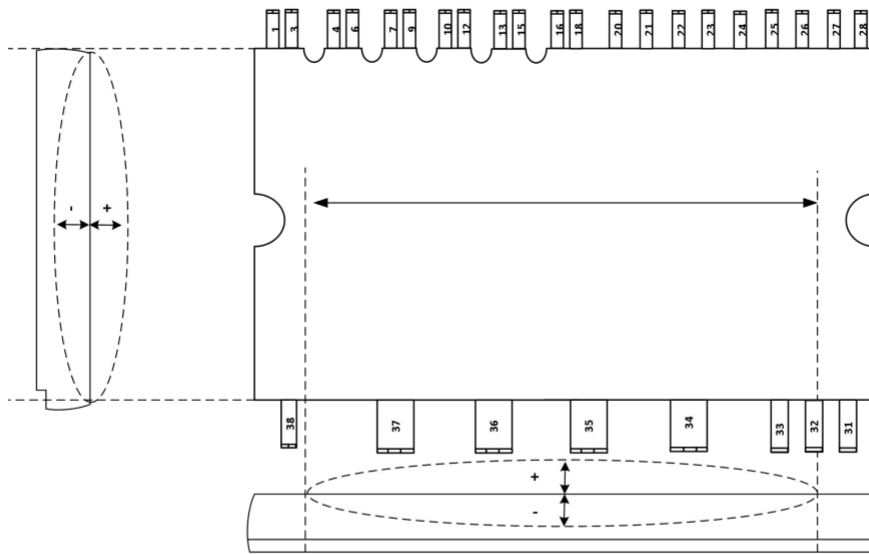


Figure 8 Flatness measurement point

APPLICATION GUIDE

ENHANCED INPUT FILTERING

Enhanced filters can improve the consistency of input/output pulses in the internal modules of HVIC and help filter out spike interference signals and narrow pulses. Below is a demonstration of classic and enhanced input filters .

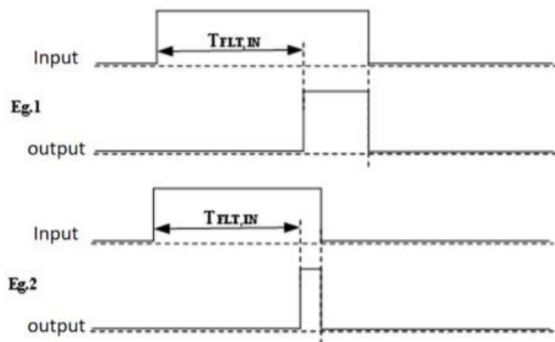


Figure 9 classic input filter

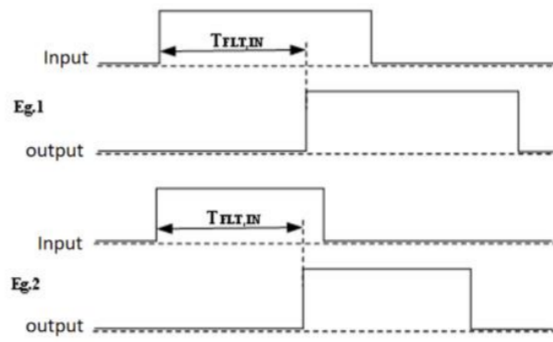


Figure 10 enhanced input filter

UNDER -VOLTAGE PROTECTION

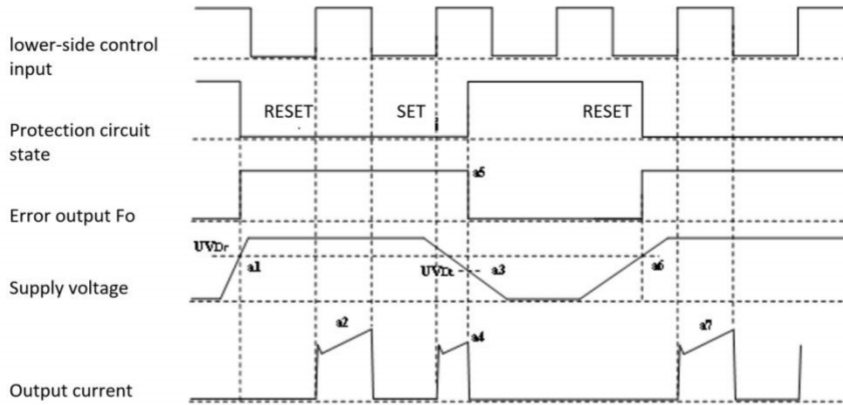


Figure 11 Under-voltage protection timing charts (N-side)

- a1.Power supply voltage rise: when the voltage exceeds the under voltage reset level, the circuit works in normal before the next under voltage signal is executed.
- a2.Normal operation: IGBT ON and outputs current.
- a3. V_D level drops to under voltage trip level(UV_{Dt}).
- a4.All N-side IGBTs turn OFF regardless of control input condition
- a5. F_o outputs for the period set by the capacitance C_{FO} , but output is extended during V_D keeps below UV_{Dr} .
- a6. V_D level reaches UV_{Dr} .
- a7.Normal operation: IGBT ON and outputs current.

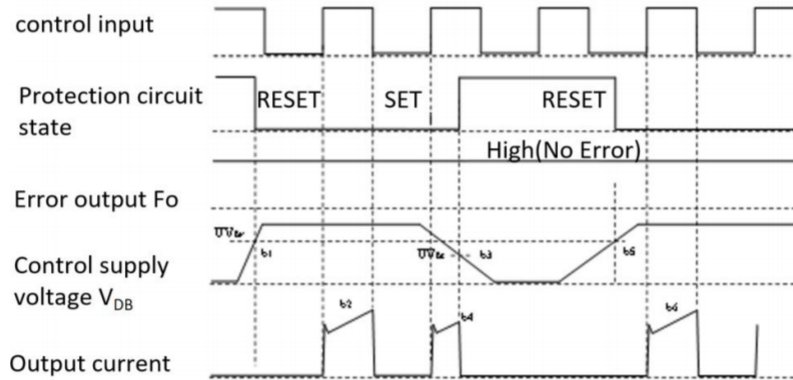


Figure 12 Under-voltage protection timing charts(P-side)

- b1. Control supply voltage V_{DB} rises: after the voltage reaches under voltage reset level UV_{Dr} , IGBT turns on by the next ON signal(L→H).
- b2.Normal operation: IGBT ON and outputs current.
- b3. V_{DB} level drops to under voltage trip level (UV_{Dt}).
- b4.IGBT of the correspond phase only turns OFF regardless of the input signal,but there is no F_o signal output.
- b5. V_{DB} level reaches UV_{Dr} .
- b6.Normal operation: IGBT ON and outputs current.

SHORT CIRCUIT PROTECTION

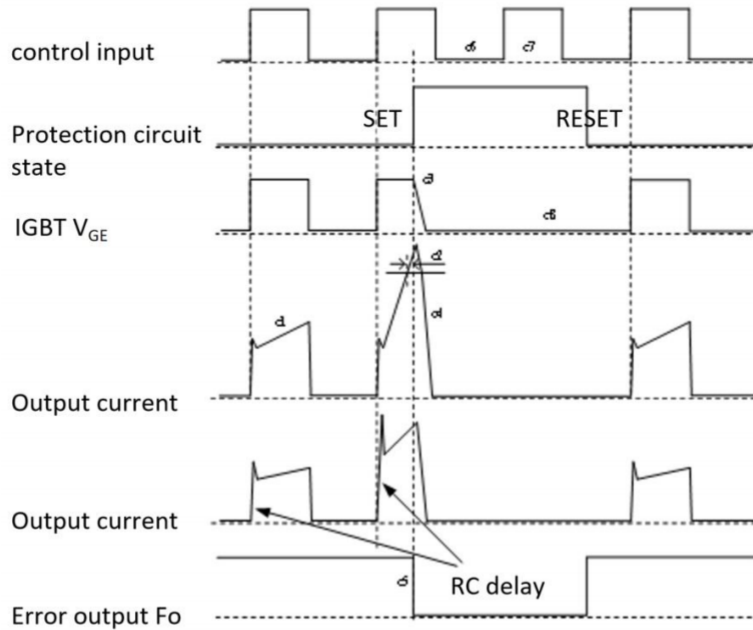


Figure 13 Short circuit protection timing charts (N-side only)

(N-side only with the external shunt resistor and RC filter)

- c1.Normal operation: IGBT ON and outputs current.
- c2.Short circuit current detection (SC trigger).
- c3.All N-side IGBT' s gates are hard interrupted .
- c4.all N-side IGBTs turn OFF.
- c5.Fo outputs. The pulse width of the Fo signal is set by the external capacitor C_{FO} .
- c6.Input= "L" : IGBT OFF.
- c7.Input= "H" : IGBT ON,in case of the Fo signal works, the IGBT still OFF.
- c8.IGBT turns off.

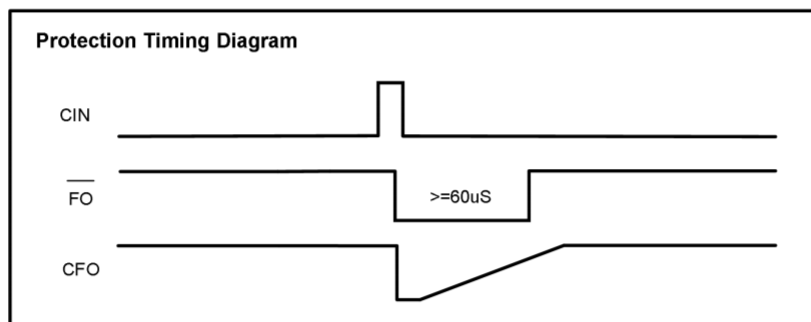


Figure 14 Over current protection timing charts

MCU I/O interface Circuit

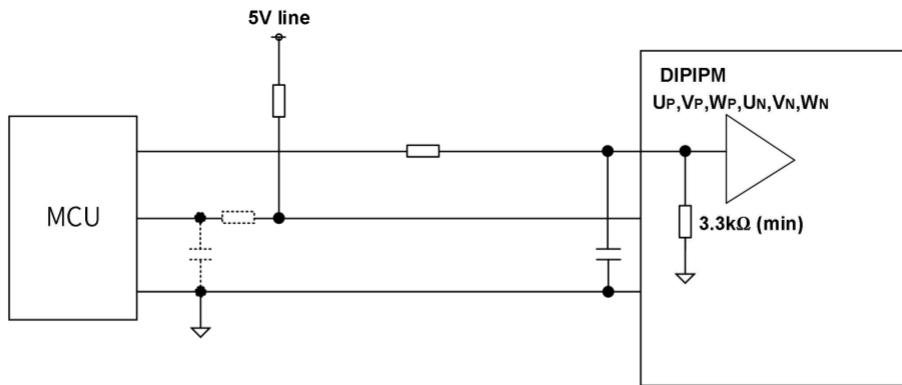


Figure 15 Recommended MCU interface circuit

Note 4: Due to the control method of PWM and the impedance of practical application circuits and PCB layout, RC decoupling may be different.

Note 5: The logical input should match the standard CMOS or TTL output.

PATTERN WIRING AROUND THE SHUNT RESISTOR

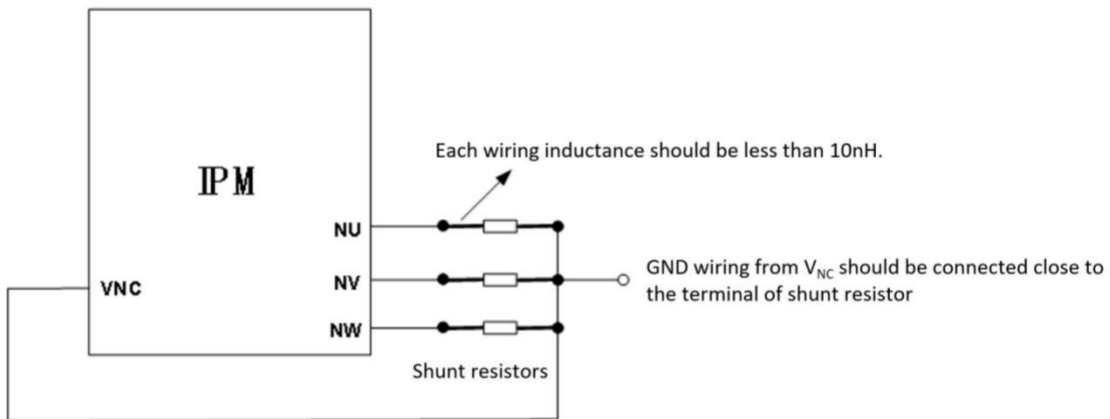


Figure 16 shunt resistor layout

TYPICAL APPLICATION CIRCUIT DIAGRAM

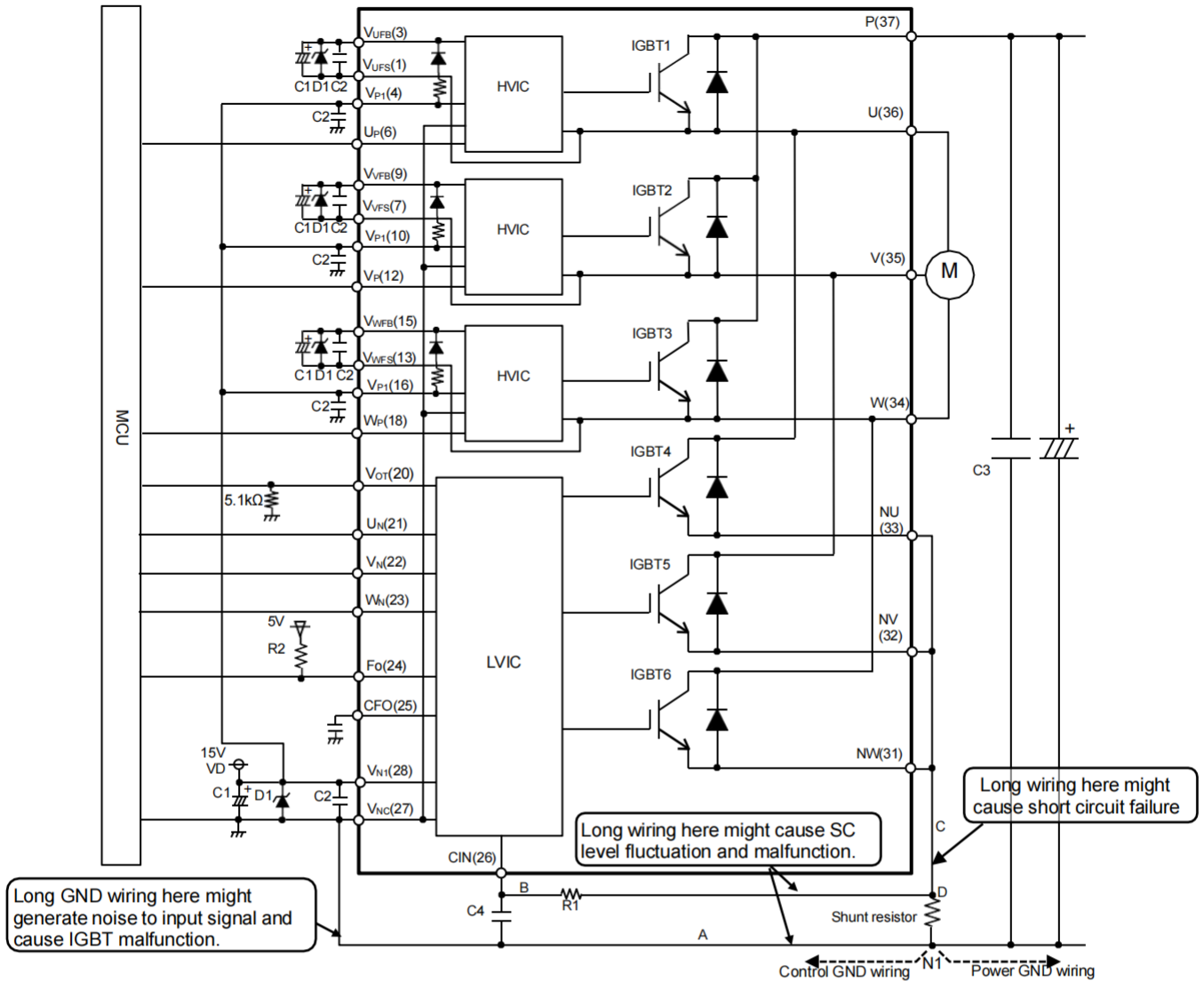


Figure 17 typical application circuit

PACKAGE OUTLINES

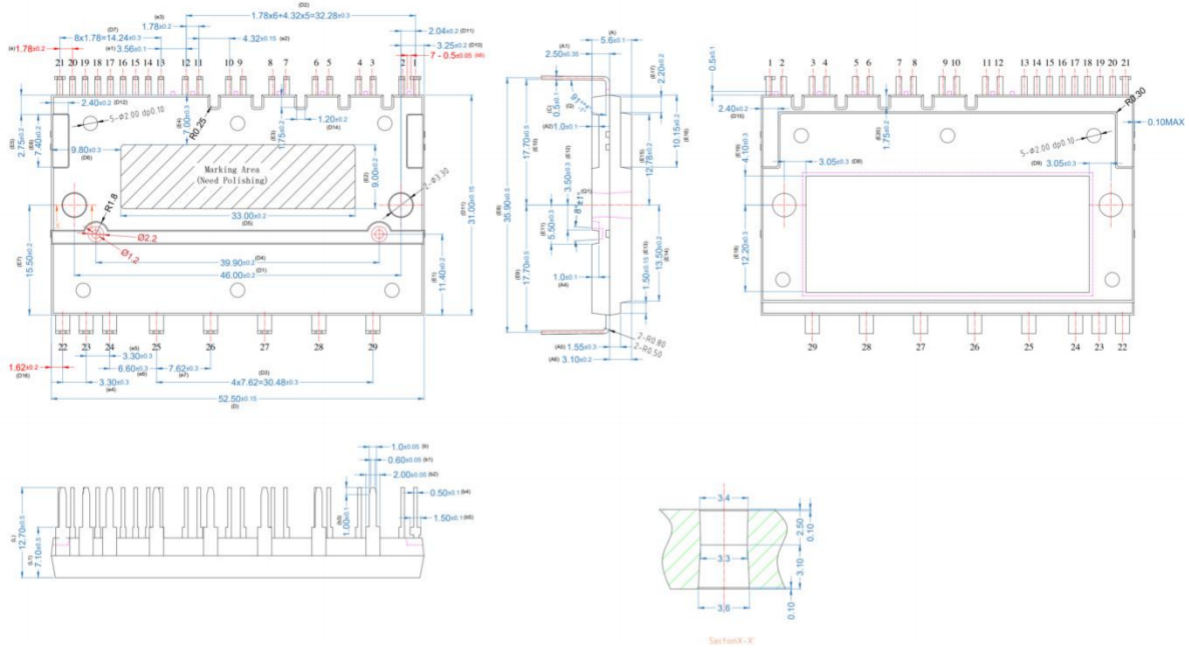


Figure 18 Package outlines

Serial Number	SYMBOL	COMMON			Serial Number	SYMBOL	COMMON			Serial Number	SYMBOL	COMMON		
		Dimensions millimeter					Dimensions millimeter					Dimensions millimeter		
		Min	Nom	Max			Min	Nom	Max			Min	Nom	Max
1	A	5.50	5.60	5.70	22	(D8)	2.75	3.05	3.35	43	(E12)	3.20	3.50	3.80
2	A1	2.15	2.50	2.85	23	(D9)	2.75	3.05	3.35	44	E13	1.35	1.50	1.65
3	A2	0.90	1.00	1.10	24	D10	3.05	3.25	3.45	45	E14	13.30	13.50	13.70
4	A4	0.90	1.00	1.10	25	D11	1.84	2.04	2.24	46	E15	12.58	12.78	12.98
5	A5	1.25	1.55	1.85	26	D12	2.20	2.40	2.60	47	E16	9.95	10.15	10.35
6	A6	2.90	3.10	3.30	27	D13	-	-	0.1	48	E17	2.00	2.20	2.40
7	b	0.95	1.00	1.05	28	D14	1.00	1.20	1.40	49	(E18)	11.90	12.20	12.50
8	b1	0.55	0.60	0.65	29	D15	2.20	2.40	2.60	50	(E19)	3.80	4.10	4.40
9	b2	1.95	2.00	2.05	30	D16	1.42	1.62	1.82	51	E20	1.55	1.75	1.95
10	b3	0.90	1.00	1.10	31	E	30.85	31.00	31.15	52	e	1.58	1.78	1.98
11	b4	0.40	0.50	0.60	32	E1	11.20	11.40	11.60	53	e1	3.46	3.56	3.66
12	b5	1.40	1.50	1.60	33	E2	8.80	9.00	9.20	54	e2	4.17	4.32	4.47
13	C	0.40	0.50	0.60	34	E3	1.55	1.75	1.95	55	e3	1.58	1.78	1.98
14	D	52.35	52.50	52.65	35	E4	6.70	7.00	7.30	56	e4	3.00	3.30	3.60
15	D1	45.80	46.00	46.20	36	E5	2.55	2.75	2.95	57	e5	3.00	3.30	3.60
16	D2	31.98	32.28	32.58	37	E6	7.20	7.40	7.60	58	e6	6.30	6.60	6.90
17	D3	30.18	30.48	30.78	38	E7	15.30	15.50	15.70	59	e7	7.32	7.62	7.92
18	D4	39.70	39.90	40.10	39	E8	35.40	35.90	36.40	60	L	12.20	12.70	13.20
19	D5	32.80	33.00	33.20	40	E9	17.20	17.70	18.20	61	L1	6.60	7.10	7.60
20	D6	9.50	9.80	10.10	41	E10	17.20	17.70	18.20	62	Q	90°	90°	95°
21	D7	13.94	14.24	14.54	42	(E11)	5.20	5.50	5.80					

Figure 19 Package dimensions

REVISE HISTORY

Date	Version	Update detail
2023. 5. 10	1. 0	Preliminary version
2023. 6. 13	1. 1	Some parameters updated
2023. 8. 14	2. 0	Some parameters updated
2023. 11. 29	3. 0	Some parameters updated
2024. 1. 31	3. 1	Revise history updated

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